Dual-Supply, 2-Bit Voltage Translator/Isolator for I²C Applications

DESCRIPTION

The SUM2102 is a high-performance configurable dual-voltage-supply translator for bi-directional voltage translation over a wide range of input and output voltages levels. The SUM2102 also works in a push-pull environment.

It is intended for use as a voltage translator between I²C-Bus compliant masters and slaves. Internal 10 kΩ pull-up resistors are provided.

The device is designed so the A port tracks the V_{CCA} level and the B port tracks the V_{CCB} level. This allows for bi-directional A/B-port voltage translation between any two levels from 1.65 V to 5.5 V. V_{CCA} can equal V_{CCB} from1.65 V to 5.5 V. Either V_{CC} can be powered-up first. Internal power-down control circuits place the device in 3-state if either V_{CC} is removed.

The two ports of the device have automatic direction-sense capability. Either port may sense an input signal and transfer it as an output signal to the other port.

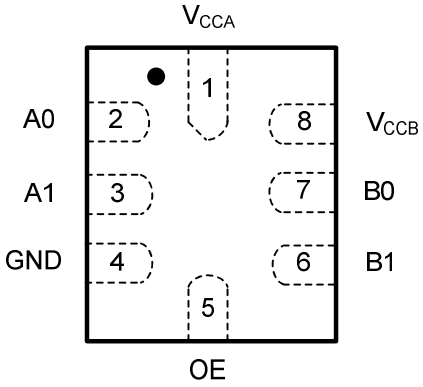
FEATURES

- Bi-Directional Interface between Any Two Levels: 1.65 V to 5.5 V
- No Direction Control Needed
- Internal 10 k Pull-Up Resistors
- System GPIO Resources Not Required when OE tied to V_{CCA}
- I²C-Bus Isolation
- A/B Port V_{OL} = 175 mV (Typical), V_{IL} = 150 mV, I_{OL} = 6 mA
- Open-Drain Inputs/Outputs
- Works in Push Pull Environment
- Accommodates Standard-Mode and Fast-Mode I²C-Bus Devices
- Supports I²C Clock Stretching & Multi-Master
- Fully Configurable: Inputs and Outputs Track V_{CC}
- Non-Preferential Power-Up; Either V_{CC} Can Power-Up First
- Outputs Switch to 3-State if Either V_{CC} is at GND
- Tolerant Output Enable: 5 V
- Package: UQFN1.2 × 1.4-8, SOT23-8
- ESD Protection Exceeds:
  - B Port: 8 kV HBM ESD (vs. GND & vs. V_{CCB})
  - All Pins: 4 kV HBM ESD (per JESD22-A114)
  - 2 kV CDM (per JESD22-C101)

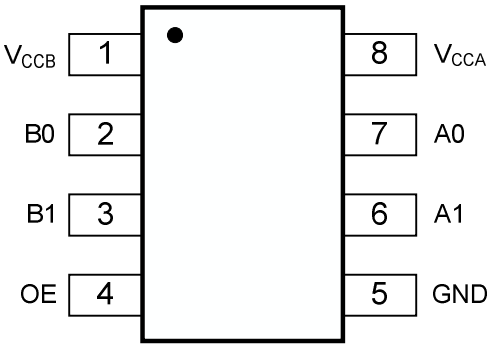
ORDER INFORMATION

Model	Package	Ordering Number	Package Quantity
SUM2102	UQFN1.2 × 1.4-8	SUM2102UQN8	Tape and Reel, 3000
	SOT23-8	SUM2102KA8	Tape and Reel, 3000

PIN CONFIGURATION (Top View)



UQFN1.2 × 1.4-8



SOT23-8

PIN DESCRIPTIONS

Pin		Symbol	Description
UQFN1.2 × 1.4-8	SOT23-8		
1	8	V_{CCA}	A-Side Power Supply
2,3	7,6	A0,A1	A-Side Inputs or 3-State Outputs
4	5	GND	Ground
5	4	OE	Output Enable port, Input
6,7	3,2	B1,B0	B-Side Inputs or 3-State Outputs
8	1	V_{CCB}	B-Side Power Supply

TRUTH TABLE

Control	Outputs
OE(1)	
LOW Logic Level	3-State
HIGH Logic Level	Normal Operation

Note:

1. If the OE pin is driven LOW, the SUM2102 is disabled and the A0, A1, B0, and B1 pins (including dynamic drivers) are forced into 3-state and all four 10 kΩ internal pull-up resisters are decoupled from their respective V_{CC}.

BLOCK DIAGRAM

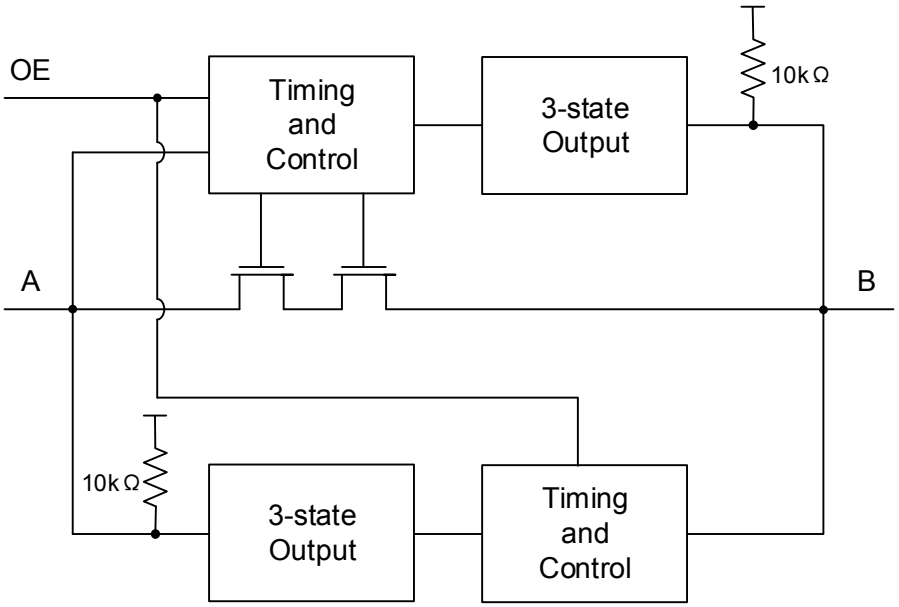


Figure 1. 1 of 2 Channels

FUNCTIONAL DESCRIPTION

Power-Up/Power-Down Sequencing

SUM2102 is a bi-directional level shift. So, translators offer an advantage in that either V_{CC} may be powered up first. This benefit derives from the chip design. When either V_{CC} is at 0 V, outputs are in a high-impedance state. The control input (OE) is designed to track the V_{CCA} supply. A pull-down resistor tying OE to GND should be used to ensure that bus contention, excessive currents, or oscillations do not occur during power-up/-down. The size of the pull-down resistor is based upon the current-sinking capability of the device driving the OE pin. We recommended the power-up and power-down as below:

The recommended power-up sequence is:

1. Apply power to the first V_{CC}.
2. Apply power to the second V_{CC}.
3. Drive the OE input HIGH to enable the device.

The recommended power-down sequence is:

1. Drive OE input LOW to disable the device.
2. Remove power from either V_{CC}.
3. Remove power from the other V_{CC}.

Note:

Alternatively, the OE pin can be hardwired to V_{CCA} to save GPIO pins. If OE is hardwired to V_{CCA}, either V_{CC} can be powered up or down first.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Min	Max	Unit
V_{CCA},V_{CCB}	Supply Voltage		-0.5	7.0	V
V_{IN}	DC Input Voltage	A Port	-0.5	7.0	
		B Port	-0.5	7.0	
		Control Input (OE)	-0.5	7.0	
V_O	Output Voltage(1)	An Outputs 3-State	-0.5	7.0	V
		Bn Outputs 3-State	-0.5	7.0	
		An Outputs Active	-0.5	V_{CCA} + 0.5 V	
		Bn Outputs Active	-0.5	V_{CCB} + 0.5 V	
I_{IK}	DC Input Diode Current	At V_{IN} < 0 V		-50	mA
I_{OK}	DC Output Diode Current	At V_O < 0 V		-50	
		At V_O > V_{CC}		+50	
I_{OH}/I_{OL}	DC Output Source/Sink Current		-50	+50	
I_{CC}	DC V_{CC} or Ground Current per Supply Pin			±100	
P_D	Power Dissipation	At 400 kHz		0.129	mW
T_{STG}	Storage Temperature Range		-65	+150	℃
ESD	Electrostatic Discharge Capability	Human Body Model, B-Port Pins		8	kV
		Human Body Model, All Pins (JESD22-A114)		4	
		Charged Device Mode, JESD22-C101		2	

Note:

Stresses beyond those listed under “ABSOLUTE MAXIMUM RATINGS” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1. I_O absolute maximum rating must be observed.

CAUTION

This integrated circuit can be damaged by ESD if you don’t pay attention to ESD protection. SUMSEMI recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

SUMSEMI reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time. Please contact SUMSEMI sales office to get the latest datasheet.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CCA}, V_{CCB}	Power Supply Operating		1.65	5.5	V
V_{IN}	Input Voltage(2)	A-Port	0	5.5	V
		B-Port	0	5.5	
		Control Input (OE)	0	V_{CCA}	
θ_{JA}	Thermal Resistance	QFN1.2 × 1.4-8		302	°C/W
T_J	Junction temperature			+150	°C
T_A	Free Air Operating Temperature		-40	+85	°C

Note:

2. All unused inputs and I/O pins must be held at V_{CCI} or GND. V_{CCI} is the V_{CC} associated with the input side.

APPLICATION CIRCUITS

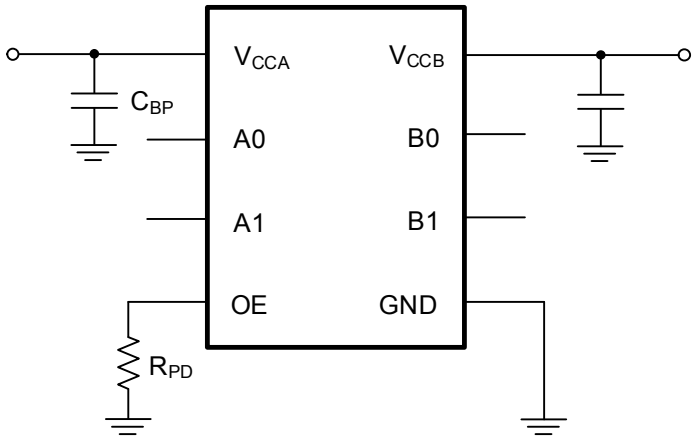


Figure 2. Application Circuit

Note: This electric circuit only supplies for reference.

APPLICATION INFORMATION

SUM2102 has open-drain I/Os and includes a total of four 10 kΩ internal pull-up resistors (R_{PU}) on each of the four data I/O pins, as shown in Figure 2. If a pair of data I/O pins (An/Bn) is not used, both pins should disconnected, eliminating unwanted current flow through the internal R_{PU}s. External R_{PU}s can be added to the I/Os to reduce the total R_{PU} value, depending on the total bus capacitance. The designer is free to lower the total pull-up resistor value to meet the maximum I^2C edge rate per the I^2C specification (UM10204 rev. 03, June 19, 2007). For example, according to the I^2C specification, the maximum edge rate (30% - 70%) during Fast Mode (400 kbit/s) is 300 ns. If the bus capacitance is approaching the maximum 400 pF, a lower total R_{PU} value helps keep the rise time below 300 ns (Fast Mode). Likewise, the I^2C specification also specifies a minimum Serial Clock Line High Time of 600 ns during Fast Mode (400 kHz). Lowering the total R_{PU} also helps increase the SCL High Time. If the bus capacitance approaches 400 pF, it may make sense to use the SUM2102, which does not contain internal $R_{PU.}$ Then calculate the ideal external R_{PU} value.

Note:

Section 7.1 of the I^2C specification provides an excellent guideline for pull-up resistor sizing.

THEORY OF OPERATION

SUM2102 is designed for high-performance level shifting and buffer / repeating in an I2C application. Figure 1 shows that each bi-directional channel contains two series-N-gates and two dynamic drivers. This hybrid architecture is highly beneficial in an I^2C application where auto-direction is a necessity.

For example, during the following three I^2C protocol events:

1. Clock Stretching
2. Slave's ACK Bit (9th bit = 0) following a Master's Write Bit (8th bit = 0)
3. Clock Synchronization and Multi-Master Arbitration

The bus direction needs to change from master-to-slave to slave-to-master without the occurrence of an edge. If there is an I^2C translator between the master and slave in these examples, the I^2C translator must change direction when both A and B ports are LOW. The N-gates can accomplish this task very efficiently because, when both A and B ports are LOW, the N-gates act as a low-resistive short between the A and B ports.

Due to I^2C's open-drain topology, I^2C masters and slaves are not push/pull drivers. Logic LOWs are "pulled down" (Isink), while logic HIGHs are "let go" (3-state). For example, when the master lets go of SCL (SCL always comes from the master), the rise time of SCL is largely determined by the RC time constant, where R = R_{PU} and C = the bus capacitance. If the SUM2102 is attached to the master [on the A port] and there is a slave on the B port, the N-gates act as a low-resistive short between both ports until either of the port's $V_{CC}/2$ thresholds are reached. After the RC time constant has reached the $V_{CC}/2$ threshold of either port, the port's edge detector triggers both dynamic drivers to drive their respective ports in the LOW-to-HIGH (LH) direction, accelerating the rising edge. Effectively, two distinct slew rates appear in rise time. The first slew rate (slower) is the RC time constant of the bus. The second slew rate (much faster) is the dynamic driver accelerating the edge.

If both the A and B ports of the translator are HIGH, a high-impedance path exists between the A and B ports because both the N-gates are turned off. If a master or slave device decides to pull SCL or SDA LOW, that device's driver pulls down (I_{sink}) SCL or SDA until the edge reaches the A or B port V_{CC}/2 threshold. When either the A or B port threshold is reached, the port's edge detector triggers both dynamic drivers to drive their respective ports in the HIGH-to-LOW (HL) direction, accelerating the falling edge.

V_{OL} vs. I_{OL}

The I^2C specification mandates a maximum V_{IL} (I_{OL} of 3 mA) of V_{CC} × 0.3 and a maximum V_{OL} of 0.4 V. If there is a master on the A port of an I^2C translator with a V_{CC} of 1.65 V and a slave on the I^2C translator B port with a V_{CC} of 3.3 V, the maximum V_{IL} of the master is (1.65 V x 0.3) 495 mV. The slave could legally transmit a valid logic LOW of 0.4 V to the master.

If the I^2C translator's channel resistance is too high, the voltage drop across the translator could present a V_{IL} to the master greater than 495 mV. To complicate matters, the I^2C specification states that 6 mA of I_{OL} is recommended for bus capacitances approaching 400 pF. More I_{OL} increases the voltage drop across the I^2C translator. The I^2C application benefits when I^2C translators exhibit low V_{OL} performance.

I^2C Bus Isolation

The SUM2102 supports I^2C-Bus isolation for the following conditions:

- ✧ Bus isolation if bus clear
- ✧ Bus isolation if either V_{CC} goes to ground

Bus Clear

Because the I^2C specification defines the minimum SCL frequency of DC, the SCL signal can be held LOW forever; however. This condition shuts down the I^2C bus. The I^2C specification refers to this condition as "Bus Clear." In Figure 3; if slave #2 holds down SCL forever, the master and slave #1 are not able to communicate because the SUM2102 passes the SCL stuck-LOW condition from slave #2 to slave #1 and as the master. However, if the OE pin is pulled LOW (disabled), both ports (A and B) are 3-stated. This results in the SUM2102 isolating slave #2 from the master and slave #1, allowing full communication between the master and slave #1.

V_{CC} to GND

If slave #2 is a camera that is suddenly removed from the I^2C bus, resulting in V_{CCB} transitioning from a valid V_{CC} (1.65 V ~ 5.5 V) to 0 V; the SUM2102 automatically forces SCL and SDA on both its A and B ports into 3-state. Once V_{CCB} has reached 0 V, full I^2C communication between the master and slave #1 remains undisturbed.

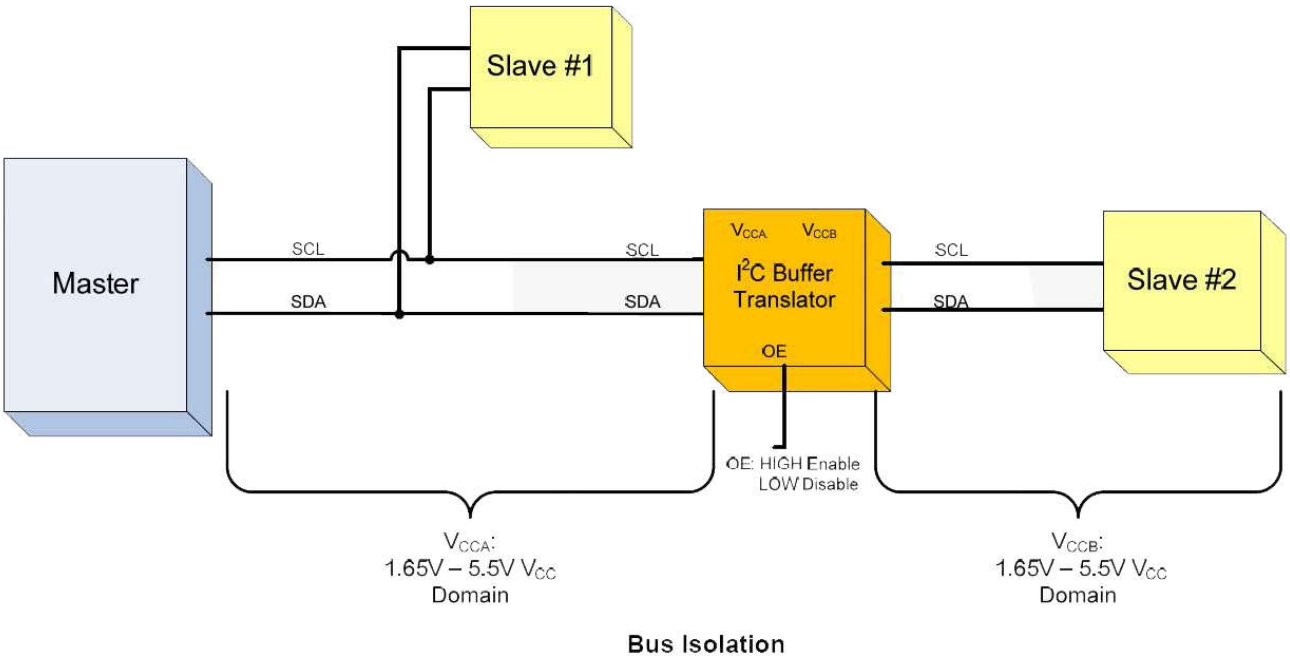


Figure 3. Bus Isolation

DC ELECTRICAL CHARACTERISTICS

T_A = –40°C to +85°C.

Symbol	Parameter	Conditions		V_{CCA}(V)	V_{CCB}(V)	Min	Typ	Max	Unit
V_{IHA}	High Level Input Voltage A	Data Inputs An		1.65~5.5	1.65~5.5	V_{CCA} - 0.4			V
		Control Input OE		1.65~5.5	1.65~5.5	0.7V_{CCA}			
V_{IHB}	High Level Input Voltage B	Data Inputs Bn		1.65~5.5	1.65~5.5	V_{CCB} - 0.4			V
V_{ILA}	Low Level Input Voltage A	Data Inputs An		1.65~5.5	1.65~5.5			0.4	V
		Control Input OE		1.65~5.5	1.65~5.5			0.3V_{CCA}	
V_{ILB}	Low Level Input Voltage B	Data Inputs Bn		1.65~5.5	1.65~5.5			0.4	V
V_{OL}	Low Level Output	V_{IL} = 0.15V		1.65~5.5	1.65~5.5			0.4	V
		I_{OL} = 6 mA							
I_L	Input Leakage Current	Control Input OE, V_{IN} = V_{CCA} or GND		1.65~5.5	1.65~5.5			±1.0	μA
I_{OFF}	Power-Off Leakage Current	An	V_{IN} or V_O = 0 V to 5.5V	0	5.5			±2.0	μA
		Bn	V_{IN} or V_O = 0 V to 5.5 V	5.5	0			±2.0	

DC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	Conditions		V_{CCA}(V)	V_{CCB}(V)	Min	Typ	Max	Unit
I_{OZ}	3-State Output Leakage (2)	An Bn	V_O = 0 V to 5.5 V, OE = V_{IL}	5.5	5.5			±2.0	μA
		An	V_O = 0 V to 5.5 V, OE = Don't care	5.5	0			±2.0	
		Bn	V_O = 0 V to 5.5 V, OE = Don't care	0	5.5			±2.0	
$I_{CCA/B}$	Quiescent Supply Current (3,4)	V_{IN} = V_{CCI} or Floating, I_O = 0		1.65 ~ 5.5	1.65 ~ 5.5			5.0	μA
I_{CCZ}	Quiescent Supply Current (3)	V_{IN} = V_{CCI} or GND, I_O = 0, OE = V_{IL}		1.65 ~ 5.5	1.65 ~ 5.5			5.0	μA
I_{CCA}	Quiescent Supply Current (2)	V_{IN} = 5.5V or GND, I_O = 0, OE = Don't Care, Bn to An		0	1.65 ~ 5.5			-2.0	μA
				1.65 ~ 5.5	0			2.0	
I_{CCB}	Quiescent Supply Current (2)	V_{IN} = 5.5V or GND, I_O = 0, OE = Don't Care, An to Bn		1.65 ~ 5.5	0			-2.0	μA
				0	1.65 ~ 5.5			2.0	
R_{PU}	Resistor Pull-up Value	V_{CCA} & V_{CCB} Sides		1.65 ~ 5.5	1.65 ~ 5.5		10		kΩ

Notes:

1. This table contains the output voltage for static conditions. Dynamic drive specifications are given in Dynamic Output Electrical Characteristics.
2. "Don't Care" indicates any valid logic level.
3. V_{CCI} is the V_{CC} associated with the input side.
4. Reflects current per supply, V_{CCA} or V_{CCB}.

DYNAMIC OUTPUT ELECTRICAL CHARACTERISTICS

Output Rise / Fall Time[5]

Output load: C_L = 50 pF, R_{PU} = NC, push / pull driver, and T_A = -40°C to +85°C.

Symbol	Parameter	V_{CCO}[6]				Unit
		4.5V to 5.5V	3.0V to 3.6V	2.3V to 2.7V	1.65V to 1.95V	
		Typ.	Typ.	Typ.	Typ.	
t_{rise}	Output Rise Time; A Port, B Port [7]	3	4	5	7	ns
t_{fall}	Output Fall Time; A Port, B Port [8]	1	1	1	1	ns

Notes:

5. Output rise and fall times guaranteed by design simulation and characterization; not production tested.
6. V_{CCO} is the V_{CC} associated with the output side.
7. See Figure 8.
8. See Figure 9.

Maximum Data Rate

Output load: C_L = 50 pF, R_{PU} = NC, push / pull driver, and T_A = -40°C to +85°C.

V_{CCA}	Direction	V_{CCB}				Unit
		4.5V to 5.5V	3.0V to 3.6V	2.3V to 2.7V	1.65V to 1.95V	
		Minimums				
4.5 V to 5.5 V	A to B	28	23	22	22	MHz
	B to A	28	26	18	10	
3.0 V to 3.6 V	A to B	26	23	19	11	MHz
	B to A	23	23	13	10	
2.3 V to 2.7 V	A to B	18	13	13	9	MHz
	B to A	22	19	13	9	
1.65 V to 1.95 V	A to B	10	10	9	8	MHz
	B to A	22	11	9	8	

Open-Drain Date Rate

V_{CCA}	Direction	V_{CCB}	Test condition	Date Rate	Unit
1.8 V ~ 5.5 V	A to B	1.8 V ~ 5.5 V	I/O port parallel 1k resistance to power supply	1	Mbps
	B to A			1	Mbps

AC CHARACTERISTICS [9]

Output Load: C_L = 50 pF, R_{PU} = NC, push / pull driver, and T_A = -40°C to +85°C.

Symbol	Parameter	V_{CCB}								Unit
		4.5 V to 5.5 V		3.0 V to 3.6 V		2.3 V to 2.7 V		1.65 V to 1.95 V		
		Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.	
V_{CCA} = 4.5 V to 5.5 V										
t_{PLH}	A to B	1	3	1	3	1	3	1	3	ns
	B to A	1	3	2	4	3	5	4	7	
t_{PHL}	A to B	2	4	3	5	4	6	5	7	ns
	B to A	2	4	2	5	2	6	5	7	
t_{PZL}	OE to A	4	5	6	10	5	9	7	15	ns
	OE to B	3	5	4	7	5	8	10	15	
t_{PLZ}	OE to A	65	100	65	105	65	105	65	105	ns
	OE to B	5	9	6	10	7	12	9	16	
V_{CCA} = 3.0 V to 3.6 V										
t_{PLH}	A to B	2.0	5.0	1.5	3.0	1.5	3.0	1.5	3.0	ns
	B to A	1.5	3.0	1.5	4.0	2.0	6.0	3.0	9.0	
t_{PHL}	A to B	2.0	4.0	2.0	4.0	2.0	5.0	3.0	5.0	ns
	B to A	2.0	4.0	2.0	4.0	2.0	5.0	3.0	5.0	
t_{PZL}	OE to A	4.0	8.0	5.0	9.0	6.0	11.0	7.0	15.0	ns
	OE to B	4.0	8.0	6.0	9.0	8.0	11.0	10.0	14.0	
t_{PLZ}	OE to A	100	115	100	115	100	115	100	115	ns
	OE to B	5	10	4	8	5	10	9	15	
t_{skew}	A Port,B Port[10]	0.5	1.5	0.5	1.0	0.5	1.0	0.5	1.0	ns

AC CHARACTERISTICS (Continued)

Symbol	Parameter	V_{CCB}								Unit
		4.5 V to 5.5 V		3.0 V to 3.6 V		2.3 V to 2.7 V		1.65 V to 1.95 V		
		Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.	
V_{CCA} = 2.3 V to 2.7 V										
t_{PLH}	A to B	2.5	5.0	2.5	5.0	2.0	4.0	1.0	3.0	ns
	B to A	1.5	3.0	2.0	4.0	3.0	6.0	5.0	10.0	
t_{PHL}	A to B	2.0	5.0	2.0	5.0	2.0	5.0	3.0	6.0	ns
	B to A	2.0	5.0	2.0	5.0	2.0	5.0	3.0	6.0	
t_{PZL}	OE to A	5.0	10.0	5.0	10.0	6.0	12.0	9.0	18.0	ns
	OE to B	4.0	8.0	4.5	9.0	5.0	10.0	9.0	18.0	
t_{PLZ}	OE to A	100	115	100	115	100	115	100	115	ns
	OE to B	65	110	62	110	65	115	12	25	
t_{skew}	A Port,B Port[10]	0.5	1.5	0.5	1.0	0.5	1.0	0.5	1.0	ns
V_{CCA} = 1.65 V to 1.95 V										
t_{PLH}	A to B	4	7	4	7	5	8	5	10	ns
	B to A	1.0	2.0	1.0	2.0	1.5	3.0	5.0	10.0	
t_{PHL}	A to B	5	8	3	7	3	7	3	7	ns
	B to A	4	8	3	7	3	7	3	7	
t_{PZL}	OE to A	11	15	11	14	14	28	14	23	ns
	OE to B	6	14	6	14	6	14	9	16	
t_{PLZ}	OE to A	75	115	75	115	75	115	75	115	ns
	OE to B	75	115	75	115	75	115	75	115	
t_{skew}	A Port,B Port[10]	0.5	1.5	0.5	1.0	0.5	1.0	0.5	1.0	ns

Notes:

9. AC characteristics are guaranteed by design and characterization.

10. Skew is the variation of propagation delay between output signals and applies only to output signals on the same port (An or Bn) and switching with the same polarity (LOW-to-HIGH or HIGH-to-LOW) (see Figure 11). Skew is guaranteed; not production tested.

CAPACITANCE

T_A = +25°C.

Symbol	Parameter	Conditions	Typ.	Unit
C_{IN}	Input Capacitance Control Pin (OE)	V_{CCA} = V_{CCB} = GND	2.2	pF
$C_{I/O}$	Input/Output Capacitance, An, Bn	V_{CCA} = V_{CCB} = 5.0 V, OE = GND	13	pF

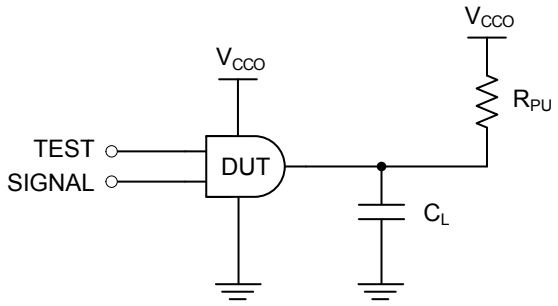


Figure 4. AC Test Circuit

Table 1. Propagation Delay Table (11)

Test	Input Signal	Output Enable Control
t_{PLH}, t_{PHL}	Data Pulses	V_{CCA}
t_{PZL} (OE to An, Bn)	0 V	LOW to HIGH Switch
t_{PLZ} (OE to An, Bn)	0 V	HIGH to LOW Switch

Note:

11. For t_{PZL} and t_{PLZ} testing, an external 2.2 kΩpull-up resister to V_{CCO} is required in order to force the I/O pins high while OE is Low because when OE is low, the internal 10 kΩ R_{PU}s are decoupled from their respective V_{CC}'s.

Table 2. AC Load Table

V_{CCO}	C_L	R_L
1.8 ± 0.15 V	50 pF	NC
2.5 ± 0.2 V	50 pF	NC
3.3 ± 0.3 V	50 pF	NC
5.0 ± 0.5 V	50 pF	NC

TIMING DIAGRAMS

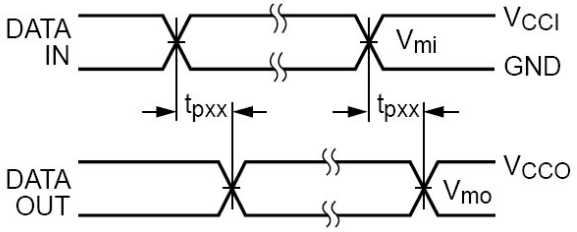


Figure 5. Waveform Inverting and Non-Inverting Functions(12)

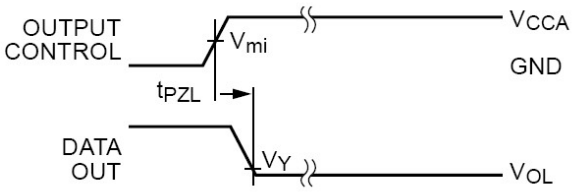
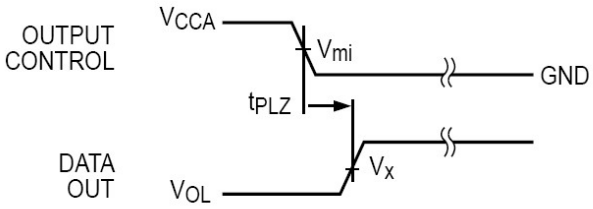


Figure 6. 3-STATE Output Low Enable Time(12)



Symbol	V_{cc}
V_{mi}(13)	V_{CCI} / 2
V_{mo}	V_{CCO} / 2
V_X	0.5 x V_{CCO}
V_Y	0.1 x V_{CCO}

Figure 7. 3-STATE Output High Enable Time(12)

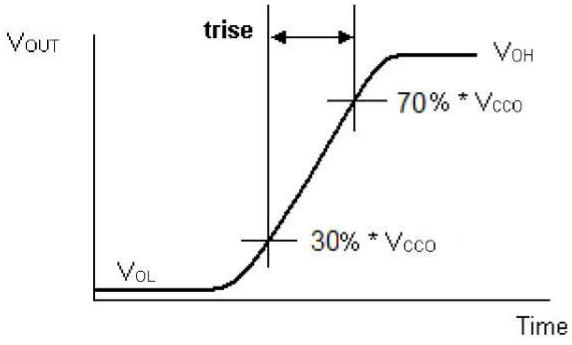


Figure 8. Active Output Rise Time

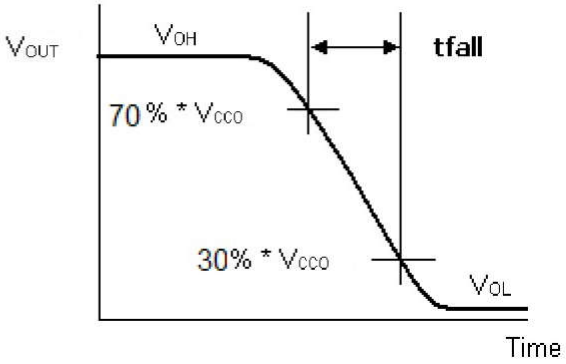


Figure 9. Active Output Fall Time

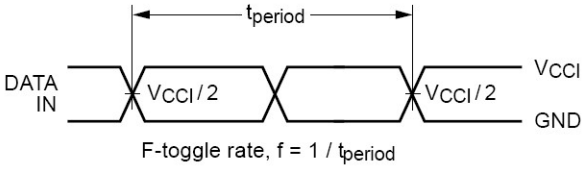


Figure 10. F-Toggle Rate

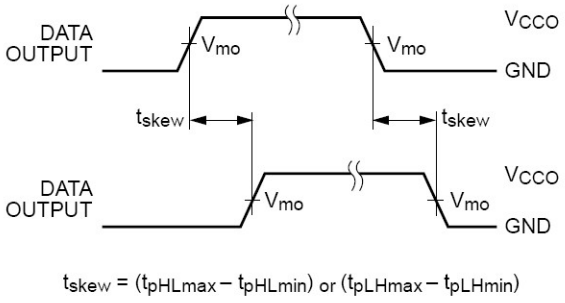


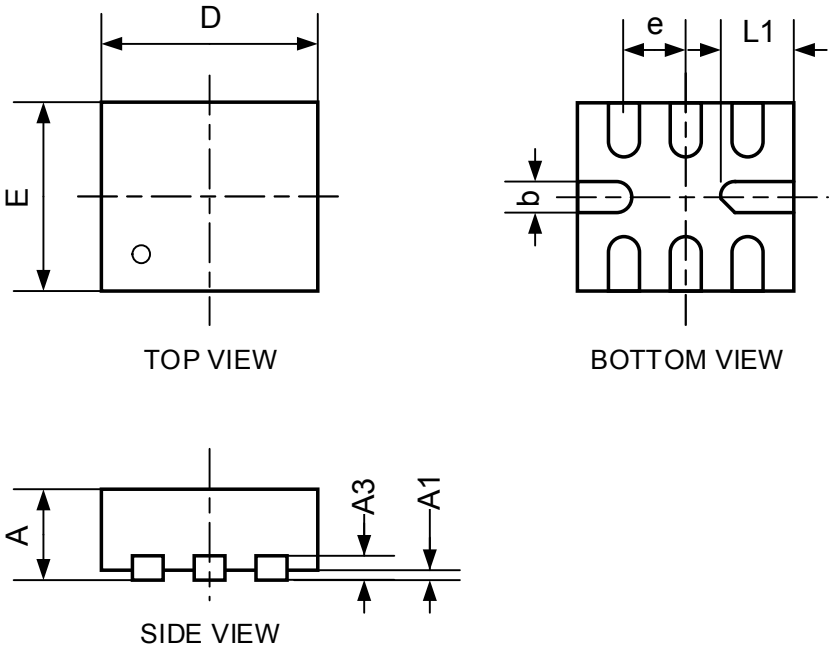
Figure 11. Output Skew Time

Notes:

12. Input $t_R = t_F$ = 2.0 ns, 10% to 90% at V_{IN} = 1.65 V to 1.95 V;
    Input $t_R = t_F$ = 2.0 ns, 10% to 90% at V_{IN} = 2.3 V to 2.7 V;
    Input $t_R = t_F$ = 2.5 ns, 10% to 90%, at V_{IN} = 3.0 V to 3.6 V only;
    Input $t_R = t_F$ = 2.5 ns, 10% to 90%, at V_{IN} = 4.5 V to 5.5 V only.
13. $V_{CCI} = V_{CCA}$ for control pin OE or Vmi = (V_{CCA} / 2).

PACKAGE OUTLINE

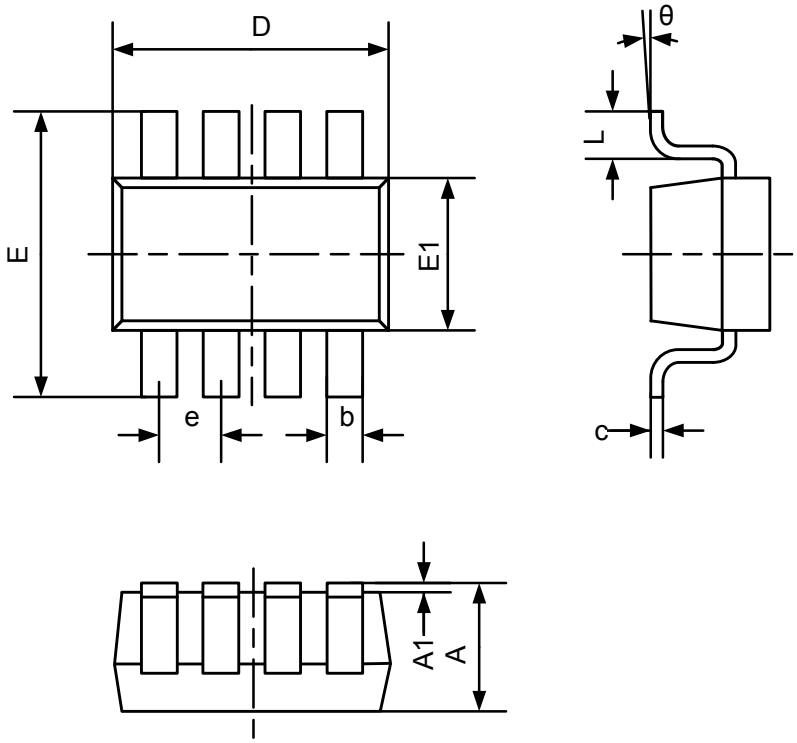
UQFN1.2 × 1.4-8



Symbol	Dimensions in Millimeters		
	Min	Nom	Max
A	0.500	0.550	0.600
A1	0.000		0.050
A3		0.150REF	
D	1.350	1.400	1.450
E	1.150	1.200	1.250
b	0.150	0.200	0.250
e		0.400BSC	
L1	0.300	0.400	0.500

PACKAGE OUTLINE

SOT23-8



Symbol	Dimensions in Millimeters	
	Min	Max
A	1.050	1.250
A1	0.000	0.100
b	0.300	0.500
c	0.100	0.200
D	2.820	3.020
E	2.650	2.950
E1	1.500	1.700
e	0.650BSC	
L	0.300	0.600
θ	0°	8°

V 1.2