Nano-Current Consumed Load Switch with Slew Rate Control

DESCRIPTION

The SUM2572 is an ultra-efficiency, 2A rated, slew rate control Load Switch. It supports the lowest quiescent current (I_Q) and shutdown current (I_{SD}) in the industry. It helps designers to reduce leakage current, improve system efficiency, and increase battery lifetime.

The SUM2572 integrated slew rate control can also enhance system reliability by mitigating bus voltage swings during switching events. The slew rate control limits the inrush current for designs with heavy capacitive loads and thereby minimizing any resulting voltage droop at the power rails.

The SUM2572 Load Switch device supports a wide input voltage range and helps to improve operating life and system robustness. Furthermore, the device supports flexible applications and can be used in multiple voltage rail applications, which helps to reduce costs.

The SUM2572 Load Switch device is small utilizing a wafer level chip scale package with 4 bumps in a 0.98 mm × 0.98 mm × 0.55 mm die size and a 0.5mm bump pitch.

FEATURES

- Low R_{ON} = 29 mΩ TYP. @ V_{IN} = 5V, T_A = 25℃
- Wide Input Range: 1.1 V to 5.5 V
- I_{OUT} Max = 2 A
- Ultra-Low I_Q: 6 nA Typ. @ V_{IN} = 5V, T_A = 25℃
- Controlled Rise Time: 340 μs @ V_{IN} = 3.3V, T_A = 25℃
- Internal EN Pull-Down Resistor
- Option for Integrated Output Discharge Switch
- Ultra-Small: 0.98 mm × 0.98 mm WLCSP
- RoHS and Green Compliant

APPLICATIONS

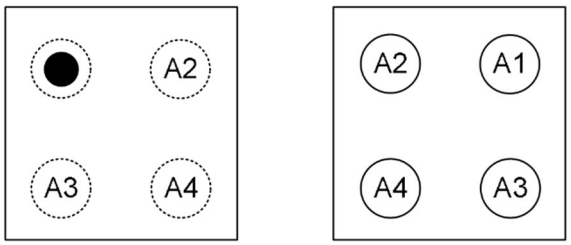
- IoT
- Wearable electronics
- SSD
- Mobile Phones
- Low Power Subsystems

ORDER INFORMATION

Model	Package	Ordering Number	Packing Option
SUM2572	WLCSP-4	SUM2572CS4	Tape and Reel

PIN CONFIGURATION (Top View)

0.98 mm × 0.98 mm WLSCP

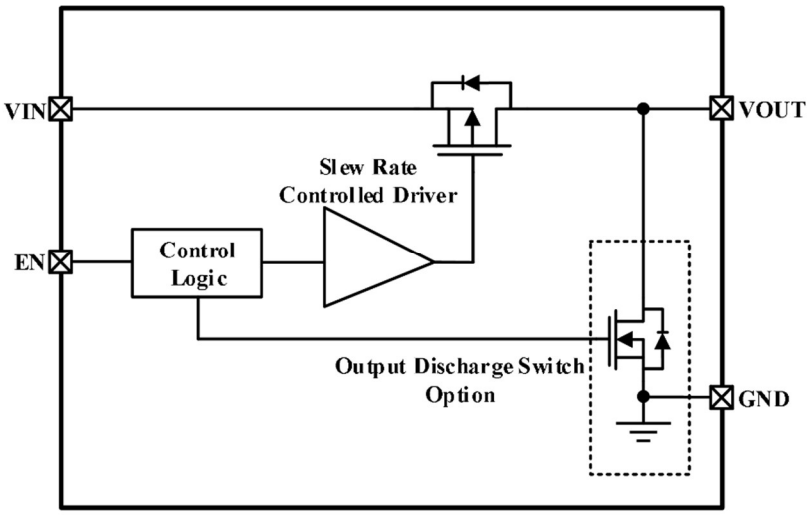


Top View Bottom View

PIN DESCRIPTIONS

Pin	Symbol	Description
A1	V_{OUT}	Switch Output
A2	V_{IN}	Switch Input. Supply Voltage for IC
A3	GND	Ground
A4	EN	Enable to control the switch

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Value	Units
V_{IN}, V_{OUT}, V_{EN}	Each Pin Voltage Range to GND	-0.3 to 6	V
I_{OUT}	Maximum Continuous Switch Current	2	A
P_D	Maximum Power Dissipation at T_A = 25°C	1	W
ESD	Human Body Model, EIA/JESD22-a114	±8	kV
	Charged Device Model, JS-002-2014	±2	
	Machine Model, EIA/JESD22-a115	±300	V
T_A	Operating Temperature Range	-40 to 85	°C
T_{STG}	Storage Temperature	-65 to 150	°C
J_A	Thermal Resistance, Junction to Ambient	110	°C/W

NOTE:

Stresses beyond those listed under “ABSOLUTE MAXIMUM RATINGS” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

This integrated circuit can be damaged by ESD if you don’t pay attention to ESD protection. SUMSEMI recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications. SUMSEMI reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time. Please contact SUMSEMI sales office to get the latest datasheet.

ELECTRICAL CHARACTERISTICS

Unless otherwise noted; V_{IN} = 3.3 V, T_A = 25°C.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Basic Operation						
V_{IN}	Supply Voltage		1.1		5.5	V
I_Q	Quiescent Current*1	I_{OUT} = 0 mA, V_{IN} = V_{EN} = 5 V		6	70	nA
		I_{OUT} = 0 mA, V_{IN} = V_{EN} = 5 V, T_A = 85°C		15		
I_{SD}	Shutdown Current	I_{OUT} = 0 mA, V_{IN} = 1.1 V, V_{EN} = 0 V		1		nA
		I_{OUT} = 0 mA, V_{IN} = 1.8 V, V_{EN} = 0 V		2		
		I_{OUT} = 0 mA, V_{IN} = 3.3 V, V_{EN} = 0 V		6	50	
		I_{OUT} = 0 mA, V_{IN} = 4.5 V, V_{EN} = 0 V		32		
		I_{OUT} = 0 mA, V_{IN} = 5 V, V_{EN} = 0 V		70		
		I_{OUT} = 0 mA, V_{IN} = 5 V, V_{EN} = 0 V, T_A = 85°C		860		
R_{ON}	On-Resistance	I_{OUT} = 100 mA, V_{IN} = V_{EN} = 1.1 V		110		mΩ
		I_{OUT} = 100 mA, V_{IN} = V_{EN} = 1.2 V		88		
		I_{OUT} = 300 mA, V_{IN} = V_{EN} = 1.8 V		50		
		I_{OUT} = 500 mA, V_{IN} = V_{EN} = 3.3 V		33	46	
		I_{OUT} = 500 mA, V_{IN} = V_{EN} = 3.3 V, T_A = 85°C		39		
		I_{OUT} = 500 mA, V_{IN} = V_{EN} = 5V		29	43	
		I_{OUT} = 500 mA, V_{IN} = V_{EN} = 5 V, T_A = 85°C		35		
R_{DSC}	Output Discharge Resistance	V_{EN} = 0 V, I_{FORCE} = 10mA	70	85	100	Ω
V_{IH}	EN Input Logic High Voltage	V_{IN} = 1.1V - 1.8V	0.9			V
		V_{IN} = 1.8V - 5.5V	1.2			V
V_{IL}	EN Input Logic Low Voltage	V_{IN} = 1.1V - 1.8V			0.3	V
		V_{IN} = 1.8V - 5.5V			0.4	V
R_{EN}	EN pull resistance	Internal Pull-Down Resistance	7	10	13	mΩ
I_{EN}	EN Current	V_{EN} = 5.5 V		0.56	0.8	μA

*1: I_Q of SUM2572 does not include the EN pin current through the pull-down or pull-up resistor $R_{EN;}$

ELECTRICAL CHARACTERISTICS

Unless otherwise noted; V_{IN} = 3.3 V, T_A = 25°C.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Switching Characteristics						
t_{dON}	Turn-On Delay*2,4	R_L = 150Ω, C_{OUT} = 0.1μF		222		μs
t_R	V_{OUT} Rise Time*2,4			340		
t_{dON}	Turn-On Delay*2,4	R_L = 510Ω, C_{OUT} = 0.1μF		211		
t_R	V_{OUT} Rise Time*2,4			378		
t_{dOFF}	Turn-Off Delay*3,4	R_L = 10Ω, C_{OUT} = 0.1μF		0.52		
t_F	V_{OUT} Fall Time*3,4			1.98		
t_{dOFF}	Turn-Off Delay*3,4	R_L = 510Ω, C_{OUT} = 0.1μF		1.22		
t_F	V_{OUT} Fall Time*3,4			16.5		

*2: t_{ON} = t_{dON} + t_R;

*3: t_{OFF} = t_{dOFF} + t_F;

*4: By design; characterized, not production tested;

ELECTRICAL PERFORMANCE

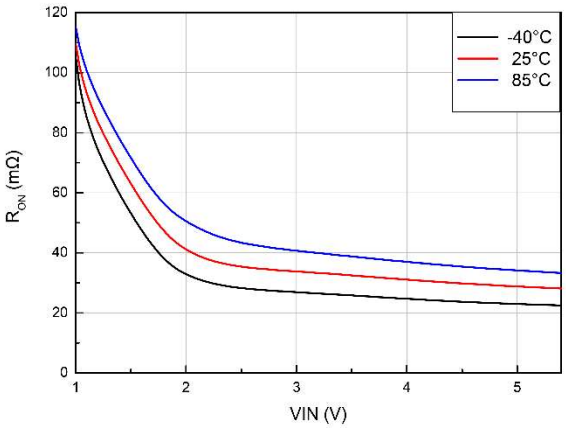


Fig. 3 R_{ON} vs. V_{IN}

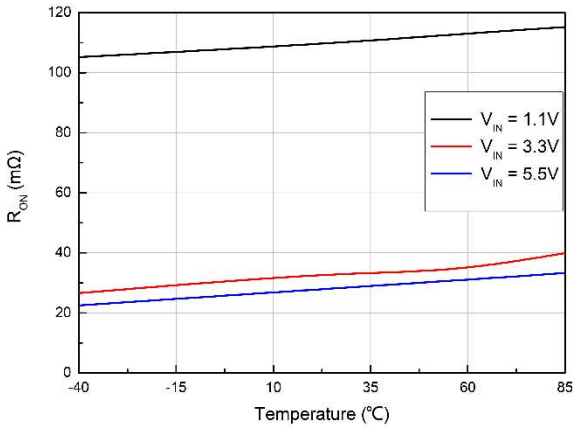


Fig. 4 R_{ON} vs. Temperature

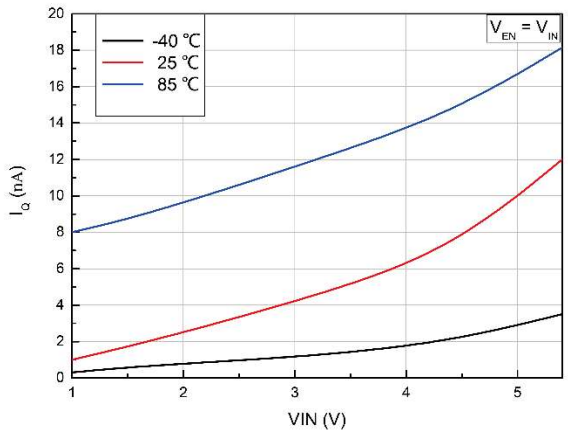


Fig. 5 I_Q vs. V_{IN}

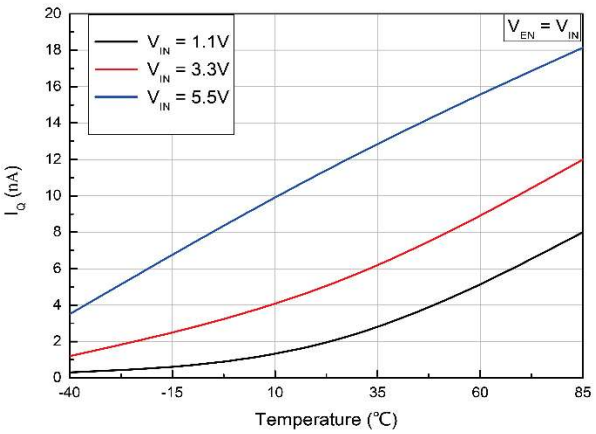


Fig. 6 I_Q vs. Temperature

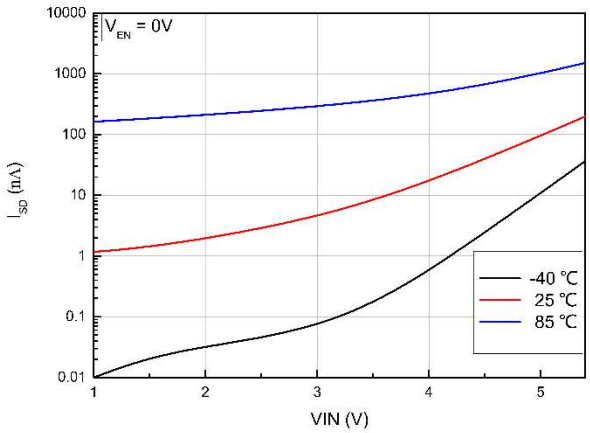


Fig. 7 I_{SD} vs. V_{IN}

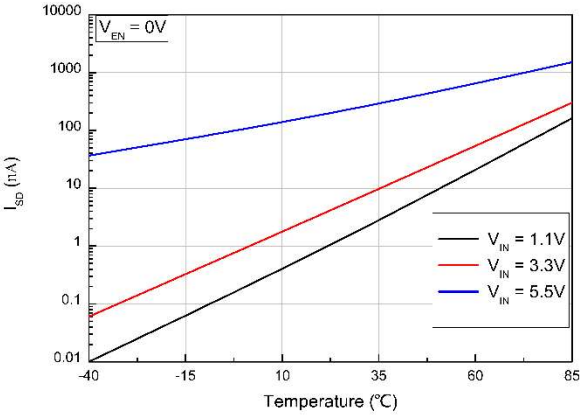


Fig. 8 I_{SD} vs. Temperature

ELECTRICAL PERFORMANCE

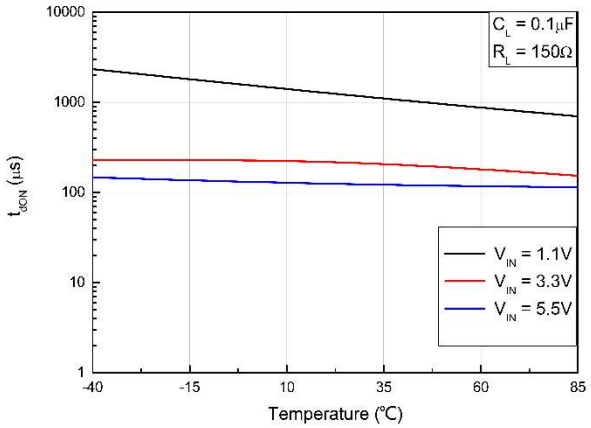


Fig. 9 t_{dON} vs. Temperature

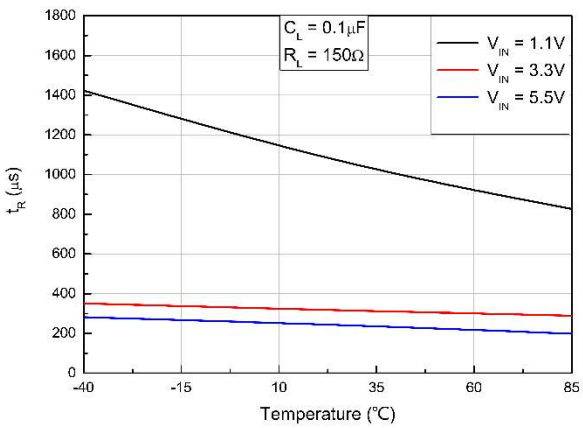


Fig. 10 t_R vs. Temperature

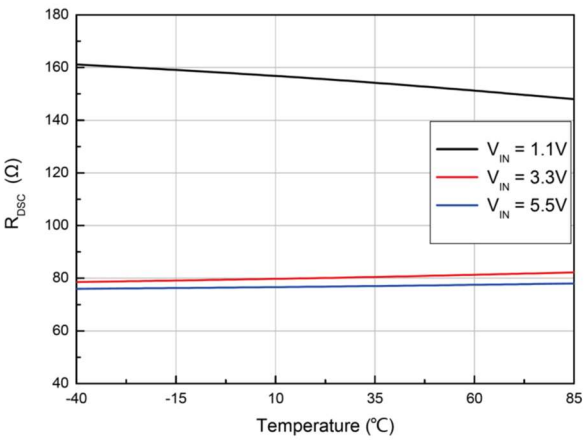


Fig. 11 R_{DSC} vs. Temperature

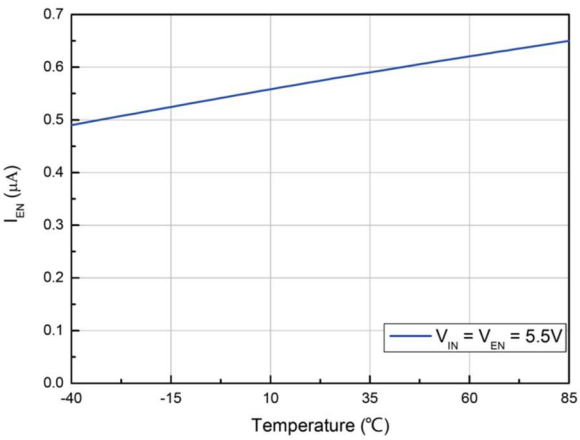


Fig. 12 I_{EN} vs. Temperature

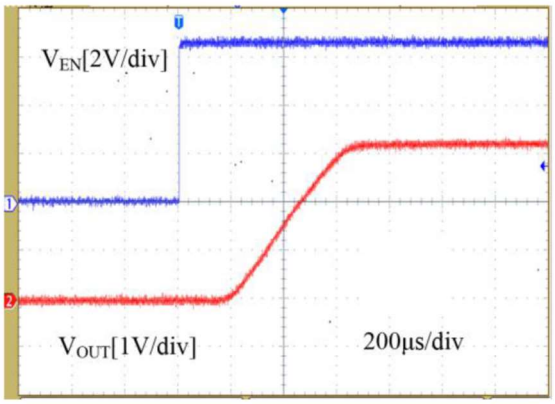


Fig. 13 Turn-On Response

V_{IN}=3.3V, C_{IN}=1μF, C_{OUT}=0.1μF, R_L=10Ω

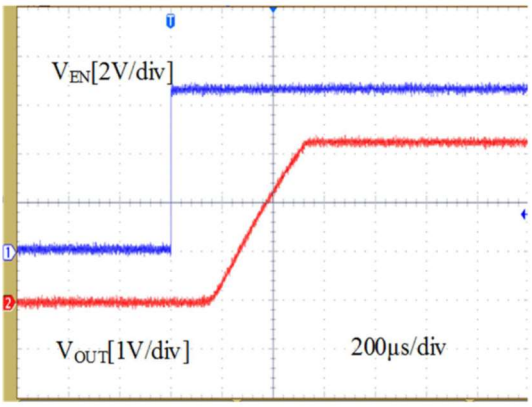


Fig. 14 Turn-On Response

V_{IN}=3.3V, C_{IN}=1μF, C_{OUT}=0.1μF, R_L=510Ω

ELECTRICAL PERFORMANCE

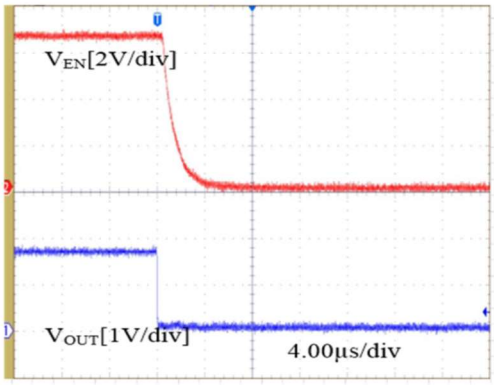


Fig. 15 Turn-Off Response

VIN=3.3V, CIN=1μF, COUT=0.1μF, RL=10Ω

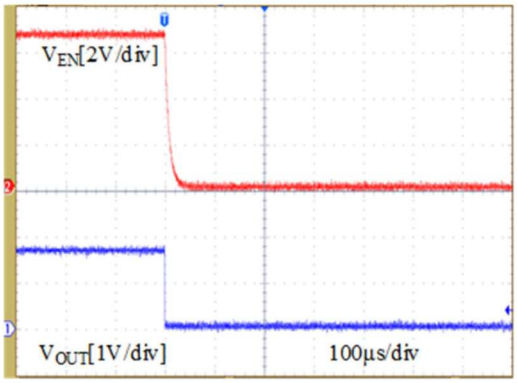
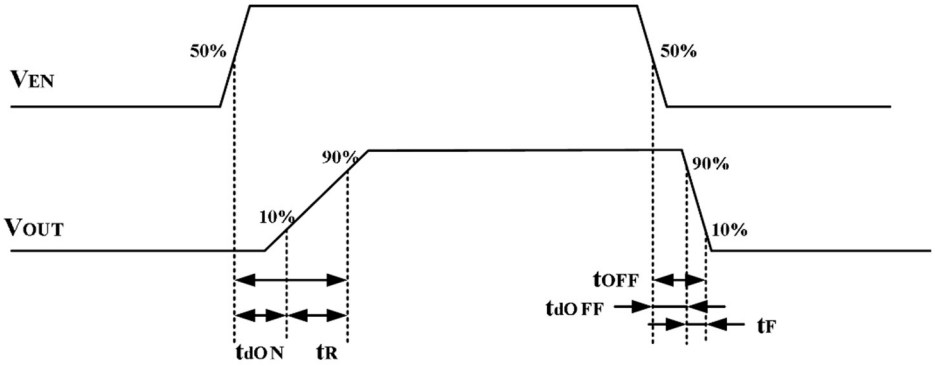


Fig. 16 Turn-Off Response

VIN=3.3V, CIN=1μF, COUT=0.1μF, RL=510Ω

TIMING DIAGRAM



APPLICATION DESCRIPTION

Input Capacitor

To limit the voltage drop on the input supply caused by transient inrush currents, an input bypass capacitor is recommended, which is recommended to be placed close to the V_{IN} pin. Higher value capacitors can further help to reduce the voltage drop.

Output Capacitor

Depending on the sink current during system start-up and system turn-off, a capacitor must be placed on the output. A 1.0μF or larger capacitor across V_{OUT} and GND pins is recommended to accommodate load transient condition. This capacitor can also help to prevent parasitic inductance which can force the output voltage to fall below GND during turn-off. Undershoot can be caused by parasitic inductance from board traces or intentional load inductances. If load inductances do exist, use of an output capacitor can improve output voltage stability and system reliability. The C_{OUT} capacitor should be placed close to the V_{OUT} and GND pins.

EN Pin

The EN pin is compatible with active HIGH GPIO and CMOS logic voltage levels and operates over the 1.1V to 5.5V operating voltage range. Note that the SUM2572 incorporates an internal pull-down resistor on the enable pin, to ensure that the device remains OFF, in the event that the pin is left floating.

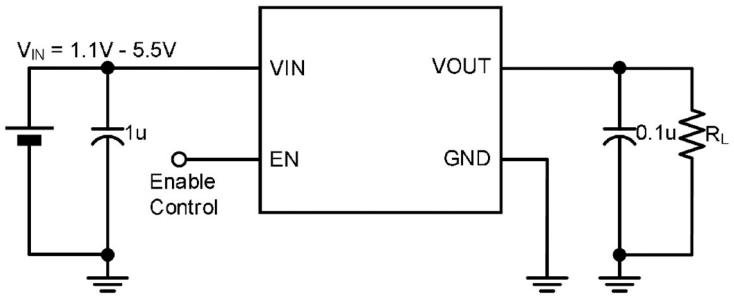
Output Discharge Function

The SUM2572(With output discharge) has an internal discharge N-channel FET switch on the V_{OUT} pin. When EN signal turns the main power FET to an off state, the N-channel switch turns on to discharge an output capacitor quickly.

Board Layout

For the best performance, all traces should be as short as possible to minimize the inductance and parasitic effects. The input and output capacitors should be kept as close as possible to the input and output pins respectively. Using wide traces for input, output, and GND help reducing the case to ambient thermal impedance.

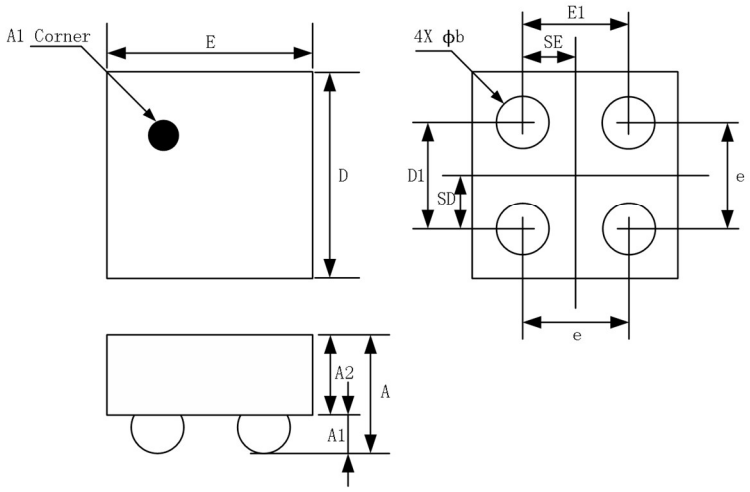
APPLICATION CIRCUITS



PACKAGE OUTLINE

WLCSP-4

0.98mm X 0.98mm WLCSP Package Outline Diagram



COMMON DIMENSIONS

(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.500	0.550	0.600
A1	0.225	0.250	0.275
A2	0.275	0.300	0.325
D	0.965	0.980	0.990
E	0.965	0.980	0.990
D1	0.450	0.500	0.550
E1	0.450	0.500	0.550
b	0.266	0.316	0.366
e	0.500 BSC		
SD	0.250 BSC		
SE	0.250 BSC		

V1.0