

1A Low Dropout LDO with Adjustable Output

DESCRIPTION

The SUM3449-ADJ series are CMOS-based low-dropout, low-power linear regulators, offering 1 A with low dropout voltage, high ripple rejection, high output accuracy and low supply current. The SUM3449-ADJ series consist of an accurate voltage-reference block, an error amplifier, a voltage-setting resistor net, a PMOSFET pass device, a thermal-shutdown circuit, and a current limit circuit with short protection.

The SUM3449-ADJ series use a type of outstanding CMOS process to minimize the supply current. A low on-resistance PMOS pass device is equipped for lower dropout voltage. SUM3449-ADJ also possess the EN function to save more energy and extend the battery life.

The SUM3449-ADJ series can choose the output current 1 A. The output voltage can be adjusted from 0.75 V to 4.3 V using two external resistors. The SUM3449-ADJ series are available in the DFN2 × 2-6 package.

FEATURES

- Wide Input Voltage Range: 1.8 V to 5.5 V
- Output Current: 1 A optional
- Adjustable Output Voltage Range: 0.75 V to 4.3 V
- Very Low I_Q : 110 μ A
- Excellent Load/Line Transient Response
- Line Regulation: 0.02% typical
- Built-in overcurrent protection and thermal shutdown circuit
- Built-in Auto-discharging circuit
- Reverse Current Protection
- Package: DFN2 × 2-6

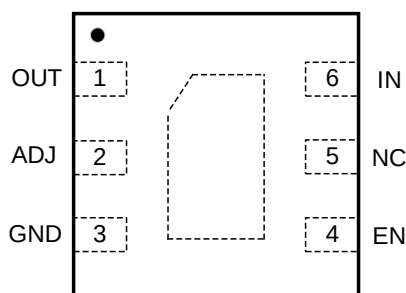
APPLICATION

- Constant-voltage power supply for battery-powered device
- Constant-voltage power supply for TV, notebook PC and home electric appliance
- Constant-voltage power supply for portable equipment
- Label Information

ORDER INFORMATION

Model	Package	Ordering Number	Packing Option
SUM3449-ADJ	DFN2 × 2-6	SUM3449-ADJUDE6	Tape and Reel, 3000

PIN CONFIGURATION (Top View)

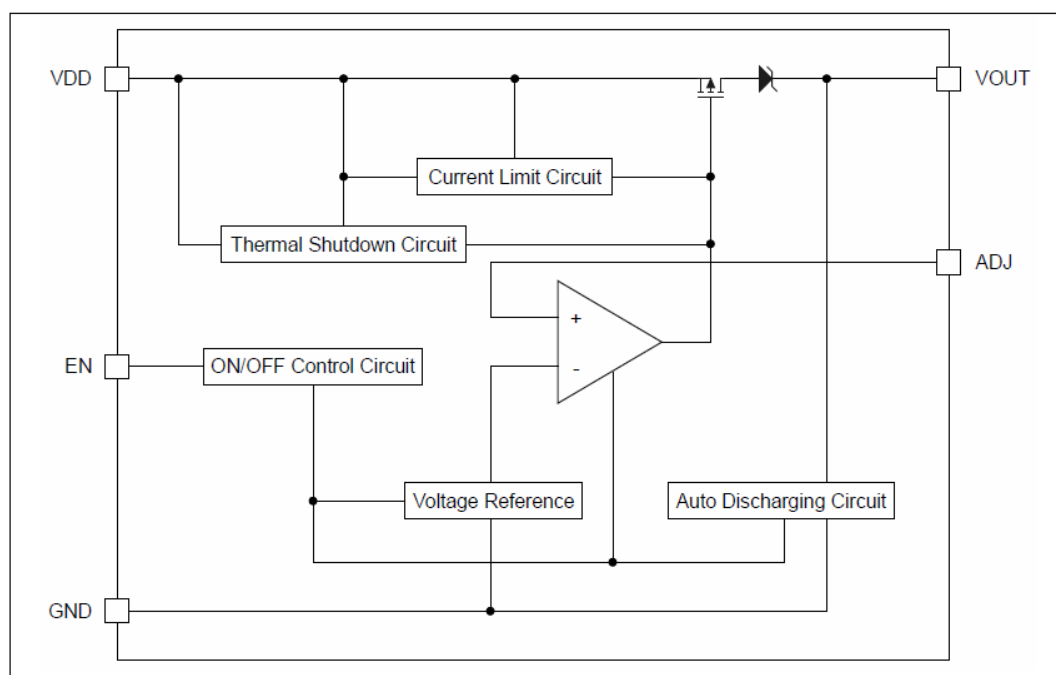


DFN2 × 2-6

PIN DESCRIPTIONS

Pin	Symbol	Description
DFN2 × 2-6		
1	OUT	Output Pin
2	ADJ	Adjustable Regulator Feedback Input. Connect to output voltage resistor divider central node.
3	GND	Ground Pin
4	EN	Chip Enable Pin
5	NC	No Connect
6	IN	Input Pin

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Input Capacitor

A 1 μ F ceramic capacitor is recommended to connect between IN and GND pins to decouple input power supply glitch and noise. The amount of the capacitance may be increased without limit. This input capacitor must be located as close as possible to the device to assure input stability and less noise. For PCB layout, a wide copper trace is required for both IN and GND.

Please pay attention, in the case of high impedance of the power supply, the input capacitance of the IC is small or the capacitor is not connected, the oscillation may occur. When the capacitance value of the output capacitor is greater than the capacitance value of the input capacitor, it is possible to generate oscillation.

Output Capacitor

An output capacitor is required for the stability of the LDO. The recommended output capacitance is 1 μ F, ceramic capacitor is recommended, and temperature characteristics are X7R or X5R. Higher capacitance values help to improve load/line transient response. The output capacitance may be increased to keep low undershoot/overshoot. Place output capacitor as close as possible to OUT and GND pins.

EN Pin Operation

The SUM3449-ADJ is turned on by setting the EN pin to “H”. When the EN pin is used, connect the EN pin with VDD to keep the LDO in operating mode.

Current Limit Protection

When output current of OUT pin is higher than current limit threshold or the OUT pin is direct short to GND, the current limit protection will be triggered and clamp the output current at a predesigned level to prevent over-current and thermal damage. SUM3449-ADJ output current limit will be 1.4 A.

Thermal Shutdown Protection

Thermal protection disables the output when the junction temperature rises to approximately +155°C, allowing the device to cool down. When the junction temperature reduces to approximately +120°C the output circuit is enabled again. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the heat dissipation of the regulator, protecting it from damage due to overheating.

Auto Discharging

When the EN pin set to “L”, the output circuit will be disable immediately, and the Auto-Discharging circuit will be turned on to discharge the electric charge on output capacitor, and decrease the voltage of OUT in very short time. The Auto-Discharging function is optional.

Reverse Current Protection Circuit

If V_{OUT} is higher than V_{IN} , the parasitic diode of Pch output transistor becomes forward direction. As a result, the current flows from OUT pin to IN pin.

The SUM3449-ADJ series switches the mode to the reverse current protection mode before V_{IN} becomes lower than V_{OUT} by connecting the parasitic diode of Pch output transistor to the backward direction, and connecting the gate to OUT pin. As a result, the Pch output transistor is turned off. However, from OUT pin to GND pin, via the internal divider resistors, very small current I_{REV} flows.

Output Voltage

The output voltage is adjustable using external 2-resistors. For better performance of the circuit, the R2 value need to be between 30k Ω and 100k Ω . The output voltage is calculated by:

$$V_{OUT} = (1+R1/R2)*0.75 (V)$$

RECOMMENDED OPERATING CONDITIONS

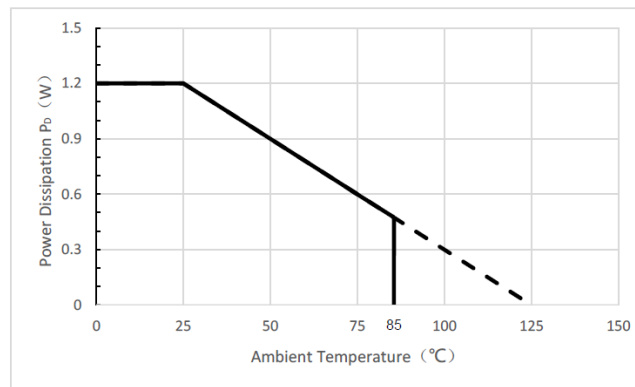
Parameter	Rating	Unit
Operating Temperature Range	-40 to +85	°C

ABSOLUTE MAXIMUM RATINGS

Symbol	Item	Rating	Unit
V_{IN}	Input Voltage	-0.3 to 6.0	V
V_{EN}	Input Voltage (EN Pin)	-0.3 to 6.0	V
V_{OUT}	Output Voltage	-0.3 to $V_{IN} + 0.3$	V
I_{MAX}	Maximum Load Current	1000	mA
P_D	Maximum Power Consumption	1200	mW
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, $T_A = 25^{\circ}\text{C}$	83	°C/W
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature Range	-65 to +150	°C
T_{SOLD}	Lead Temperature (Soldering, 5sec)	260	°C
ESD	Reference: ESDA/JEDEC JS-001-2017 (HBM)	±4000	V
	Reference: ESDA/JEDEC JS-002-2014 (CDM)	±1500	

NOTE:

Stresses beyond those listed under "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



Power Dissipation

CAUTION

This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. SUMSEMI recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

SUMSEMI reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time. Please contact SUMSEMI sales office to get the latest datasheet.

ELECTRICAL CHARACTERISTICS

$V_{IN} = V_{SET} + 1.0\text{ V}$, $I_{OUT} = 1\text{ mA}$, $C_{IN} = C_{OUT} = 1\text{ }\mu\text{F}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Operation Range	$V_{IN}^{(1)}$	$V_{IN} \geq V_{SET} + 0.5\text{ V}$	1.8		5.5	V
Output Voltage	V_{OUT}	$I_{OUT} = 1\text{ mA}$, $T_A = 25^\circ\text{C}$	$\times 0.98$		$\times 1.02$	V
		$I_{OUT} = 1\text{ mA} \sim 1\text{ A}$, $T_A = 25^\circ\text{C}$	-30		+30	mV
Dropout Voltage	$V_{DROP}^{(2)}$	$V_{OUT} = 3.3\text{ V}$, $I_{OUT} = 1\text{ A}$, V_{OUT} dropping to $0.98 \times V_{OUT}$	60	135	210	mV
Supply Quiescent Current	I_{Q_ON}	Active mode: $V_{EN} = \text{high}$. $I_{OUT} = 0\text{ mA}$	70	110	150	μA
Supply Shutdown Current	I_{Q_OFF}	$V_{EN} = 0\text{ V}$		1	3	μA
Output Voltage Line Regulation	Reg_{LINE}	$V_{SET} + 0.5\text{ V} \leq V_{IN} \leq 5.5\text{ V}$ ($V_{IN} \geq 1.8\text{ V}$), $I_{OUT} = 10\text{ mA}$ ($\Delta V_{OUT}/\Delta V_{IN}/V_{OUT}$)		0.02	0.1	%/V
Output Voltage Load Regulation	Reg_{LOAD}	I_{OUT} from 1 mA to 1 A $V_{IN} = V_{SET} + 0.5\text{ V} (\Delta V_{OUT})$		5	30	mV
Line Transient (The absolute value of the output change)	$V_{TRLN}^{(3)}$	$V_{OUT} = 3.3\text{ V}$, $I_{OUT} = 1\text{ mA}$, $V_{IN} = 4.3\text{ V}$ to 5.5 V in $10\text{ }\mu\text{s}$, $T_A = 25^\circ\text{C}$		15	30	mv
		$V_{OUT} = 3.3\text{ V}$, $I_{OUT} = 1\text{ mA}$, $V_{IN} = 5.5\text{ V}$ to 4.3 V in $10\text{ }\mu\text{s}$, $T_A = 25^\circ\text{C}$		15	30	
Load Transient (The absolute value of the output change)	$V_{TRLD}^{(3)}$	$V_{OUT} = 3.3\text{ V}$, $V_{IN} = 4.3\text{ V}$, I_{OUT} from 1 mA to 1000 mA in $10\text{ }\mu\text{s}$, $T_A = 25^\circ\text{C}$		75	120	mv
		$V_{OUT} = 3.3\text{ V}$, $V_{IN} = 4.3\text{ V}$, I_{OUT} from 1000 mA to 1 mA in $10\text{ }\mu\text{s}$, $T_A = 25^\circ\text{C}$		75	120	
Output Current	I_{OUT}		1000			mA
Max Output Instant Current	$I_{INSTANT}^{(3)}$	$V_{OUT} = 3.3\text{ V}$, $V_{IN} = 4.3\text{ V}$, $T_A = 25^\circ\text{C}$	1500			mA
Short Current Limit	I_{SHORT}	$V_{OUT} = 0\text{ V}$, $T_A = 25^\circ\text{C}$	60	130	200	mA
Inrush Current Limit	I_{RUSH}	$V_{OUT} = 3.3\text{ V}$, $V_{IN} = 4.3\text{ V}$, $T_A = 25^\circ\text{C}$	400	600	800	mA
Power Supply Rejection Ratio	$\text{PSRR}^{(3)}$	$f = 1\text{ kHz}$, $C_{OUT} = 1\text{ }\mu\text{F}$, $I_{OUT} = 20\text{ mA}$, $V_{IN} = 4.3\text{ V}$, $T_A = 25^\circ\text{C}$		70		dB

ELECTRICAL CHARACTERISTICS (CONTINUED)
 $V_{IN} = V_{SET} + 1.0\text{ V}$, $I_{OUT} = 1\text{ mA}$, $C_{IN} = C_{OUT} = 1\text{ }\mu\text{F}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Noise	$e_N^{(3)}$	10 Hz to 100 kHz, $I_{OUT} = 30\text{ mA}$, $C_{OUT} = 1\text{ }\mu\text{F}$, $T_A = 25^\circ\text{C}$		50* V_{OUT}	80* V_{OUT}	μVRMS
EN Low Threshold	V_{IL}	$V_{IN} = 1.8\text{ to }5.5\text{ V}$			0.3	V
EN High Threshold	V_{IH}	$V_{IN} = 1.8\text{ to }5.5\text{ V}$	1			V
EN Pull-down Current	I_{EN}	$V_{IN} = 4.3\text{ V}$, $V_{EN} = 4.3\text{ V}$, $T_A = 25^\circ\text{C}$		0.3	1	μA
Output resistance of auto discharge at off state	R_{LOW}	$V_{EN} = 0\text{ V}$, $V_{IN} = 4\text{ V}$, $I_{OUT} = 10\text{ mA}$	30	60	100	Ω
Soft start time	T_{ON}	$V_{OUT}=3.3\text{V}$, from enable to $0.9*V_{OUT}$	40	90	180	μs
V_{OUT} rising time	T_R	$V_{OUT}=3.3\text{V}$, from $0.1*V_{OUT}$ to $0.9*V_{OUT}$	30	60	120	
Thermal Shutdown Temperature	$T_{TSD}^{(3)}$	Junction Temperature Rising	135	155	175	$^\circ\text{C}$
Thermal Shutdown Released hysteresis	$T_{HYS}^{(3)}$	Junction Temperature falling from shutdown	20	40	60	

Note (1): Here V_{IN} means internal circuit can work normal. If $V_{IN} < V_{OUT}$, Reverse current protection circuit will work.

Note (2): V_{DROP} FT test method: test the V_{OUT} voltage at $V_{SET} + V_{DROPMAX}$ with output current.

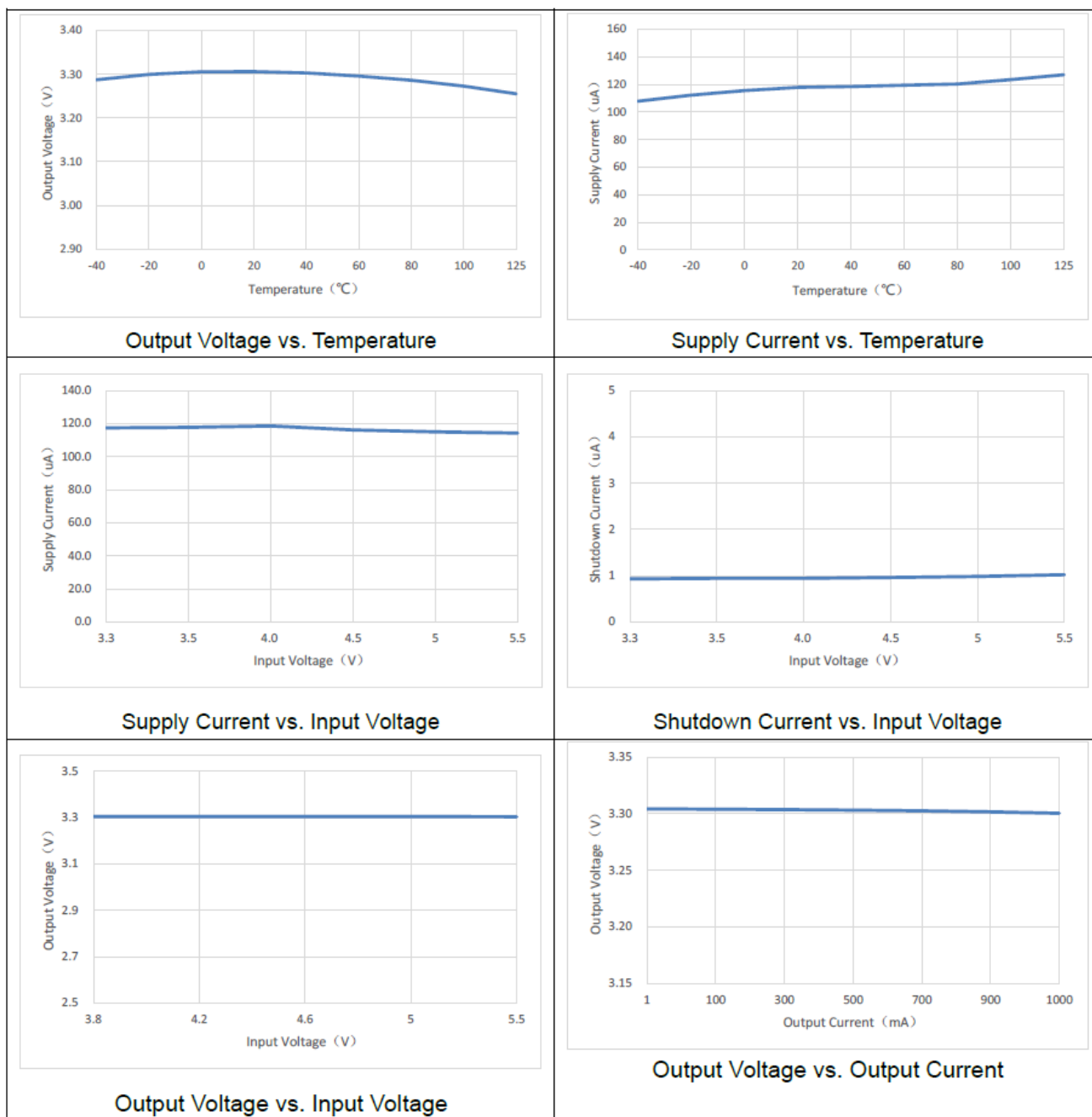
Note (3): Guaranteed by design and characterization. Not a FT item.

Note (4): Effective capacitance, including the effect of DC bias, tolerance and temperature.

TYPICAL CHARACTERISTICS

(Unless otherwise noted, $V_{IN} = V_{SET} + 1.0\text{ V}$, $T_A = -40^\circ\text{C} \sim 85^\circ\text{C}$, $C_{IN} = C_{OUT} = 1\text{ }\mu\text{F}$; Typical values are at $V_{IN} = V_{SET} + 1.0\text{ V}$, $T_A = 25^\circ\text{C}$)

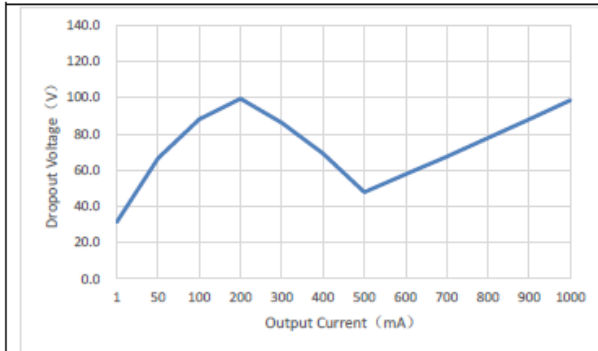
$V_{OUT} = 3.3\text{ V}$



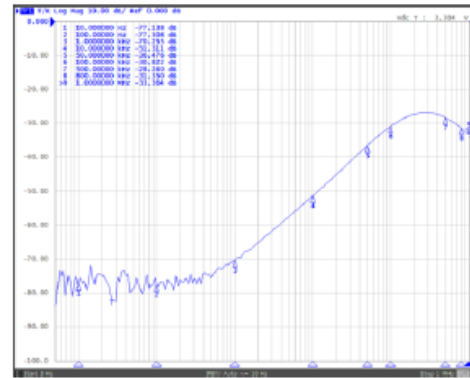
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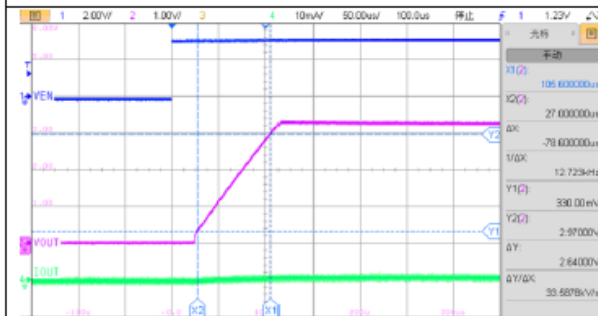
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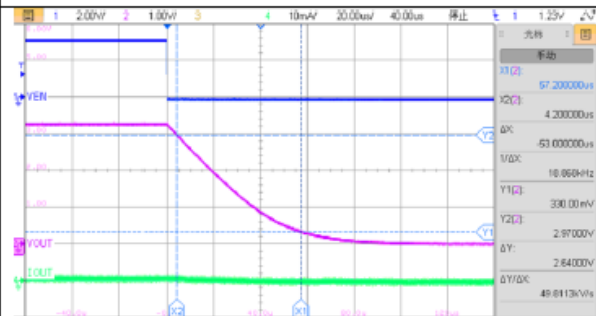
Dropout Voltage vs. Output Current



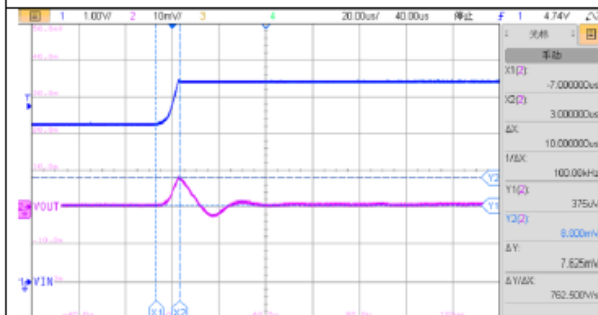
PSRR-20mA



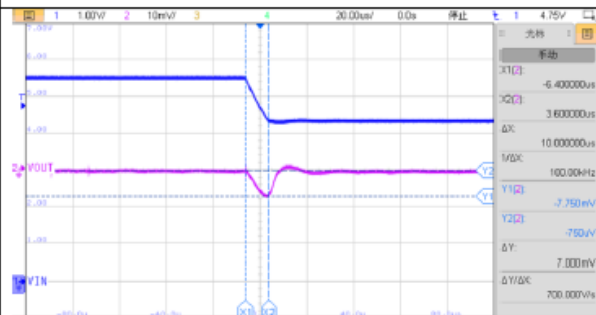
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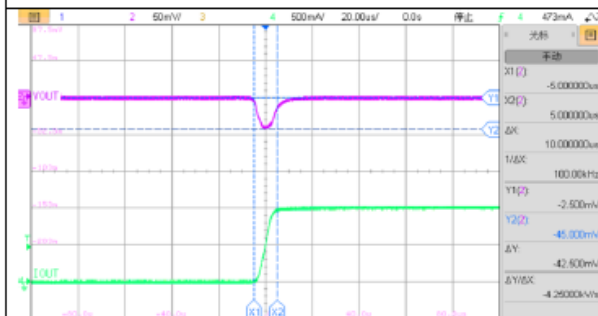
Toff



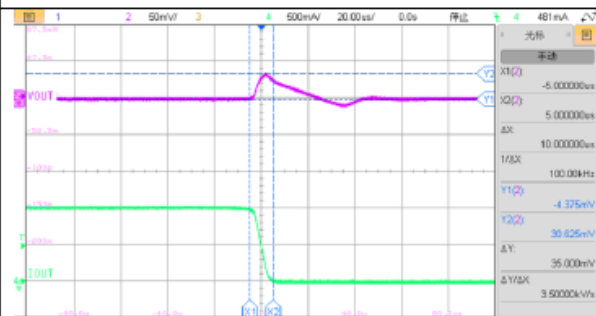
Line transient $V_{IN} = 4.3\text{ V}$ to 5.5 V



Line transient $V_{IN} = 5.5\text{ V}$ to 4.3 V

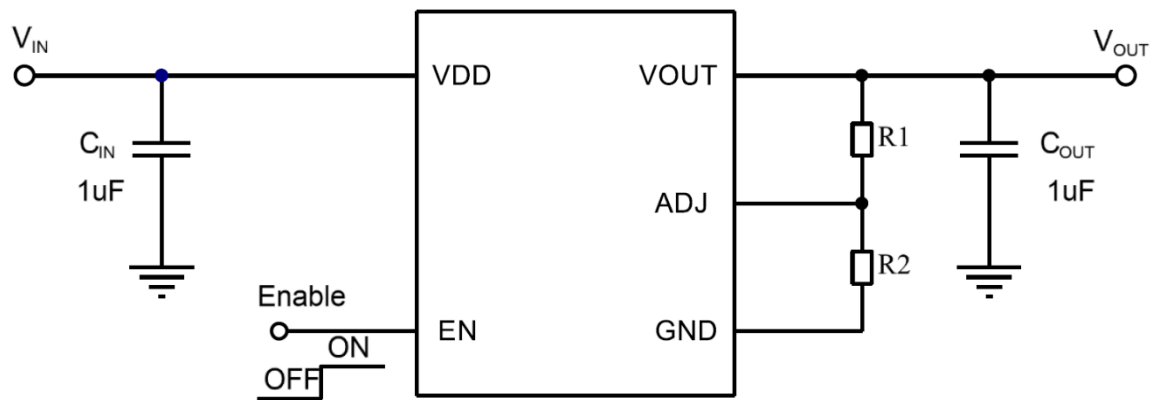


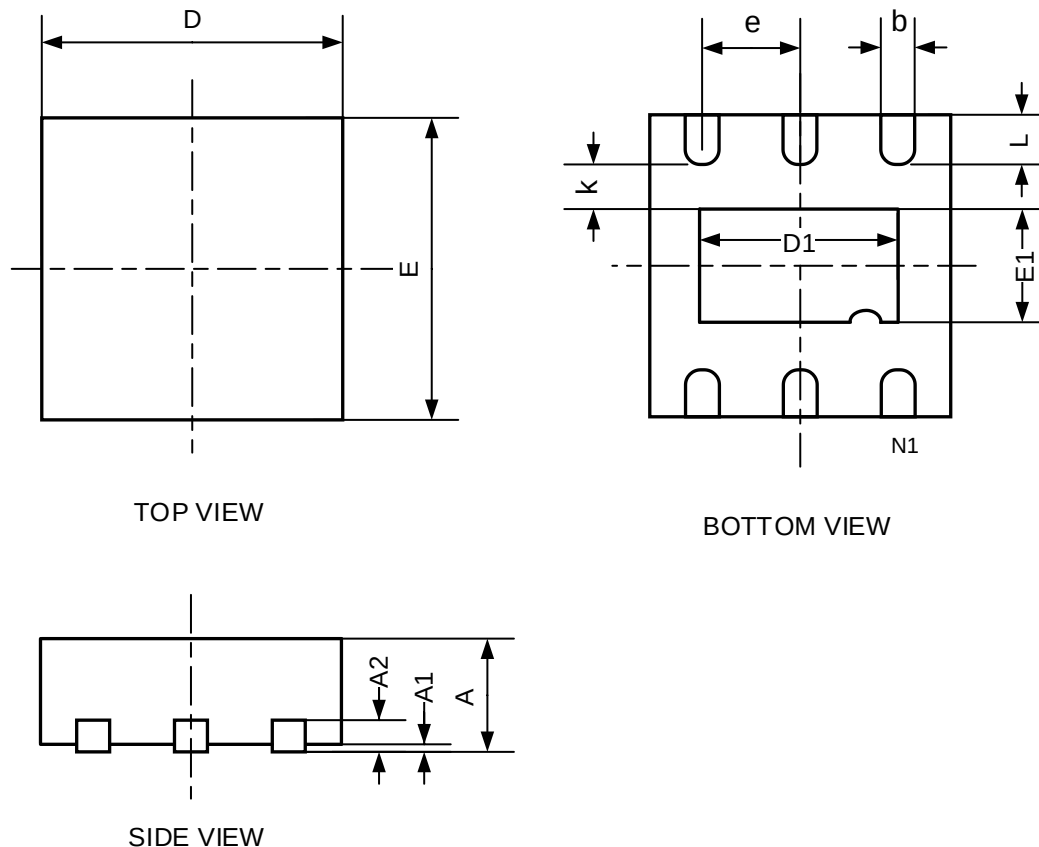
Load transient $I_{OUT} = 1\text{ mA}$ to 1 A



Load transient $I_{OUT} = 1\text{ A}$ to 1 mA

APPLICATION CIRCUITS



PACKAGE OUTLINE
DFN2 × 2-6


Symbol	Dimensions In Millimeters	
	Min	Max
A	0.700	0.900
A1	0.000	0.050
A2	0.203REF	
b	0.180	0.300
D	1.900	2.100
D1	1.100	1.300
E	1.900	2.100
E1	0.600	0.800
e	0.650BSC	
L	0.250	0.450
k	0.200	

V 1.2