500mA Ultra Low Noise LDO for RF and Analog Circuits

DESCRIPTION

The SUM3452 family of low-dropout (LDO), low-power linear regulators offers very high power supply rejection ratio (PSRR) while maintaining very low 18 μA ground current, suitable for RF applications. The family uses an advanced CMOS process and a PMOSFET pass device to achieve fast start-up, very low noise, excellent transient response, and excellent PSRR performance.

The SUM3452 is stable with a 1.0 μF ceramic output capacitor, and uses a precision voltage reference and feedback loop to achieve a worst-case accuracy of 2% over all load, line, process, and temperature variations. It is offered in a small DFN1.0 × 1.0-4, SOT23-5 and SOT89-3 package, which is ideal for small form factor portable equipment such as wireless handsets and PDAs.

FEATURES

- Wide Input Voltage Range: 2.1 V to 5.5 V
- Output Voltage : 1.2 V to 4.5 V
- Up to 500 mA Load Current
- Other Output Voltage Options Available on Request
- Very Low I_Q: 18 μA
- Low Dropout: 180 mV @ 3.3 V typical
- Very High PSRR: 76 dB at 1 kHz
- Ultra Low Noise: 20 μV_{RMS} at 3.3 V output (load = 1 mA)
- Excellent Load/Line Transient Response
- Line Regulation: 0.02%/V typical
- With Auto Discharge

APPLICATIONS

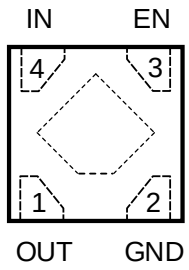
- Smart Phones and Cellular Phones
- PDAs
- MP3/MP4 Player
- Digital Still Cameras
- Portable Instrument

ORDER INFORMATION

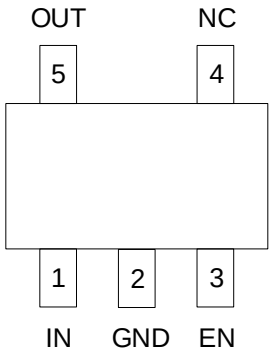
Model	Package	Ordering Number	Packing Option
SUM3452	DFN1.0 × 1.0-4	SUM3452-XXYB	Tape and Reel, 10000
	SOT23-5	SUM3452-XXKA5	Tape and Reel, 3000
	SOT89-3	SUM3452-XXP	Tape and Reel, 1000

*XX: When expressed as 18, the output voltage is 1.8V; when expressed as 30 the output voltage is 3.0V.

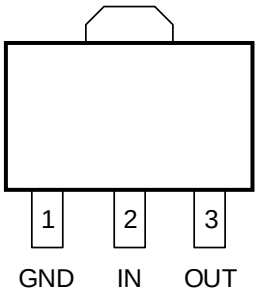
PIN CONFIGURATION (Top View)



DFN1.0 × 1.0-4



SOT23-5

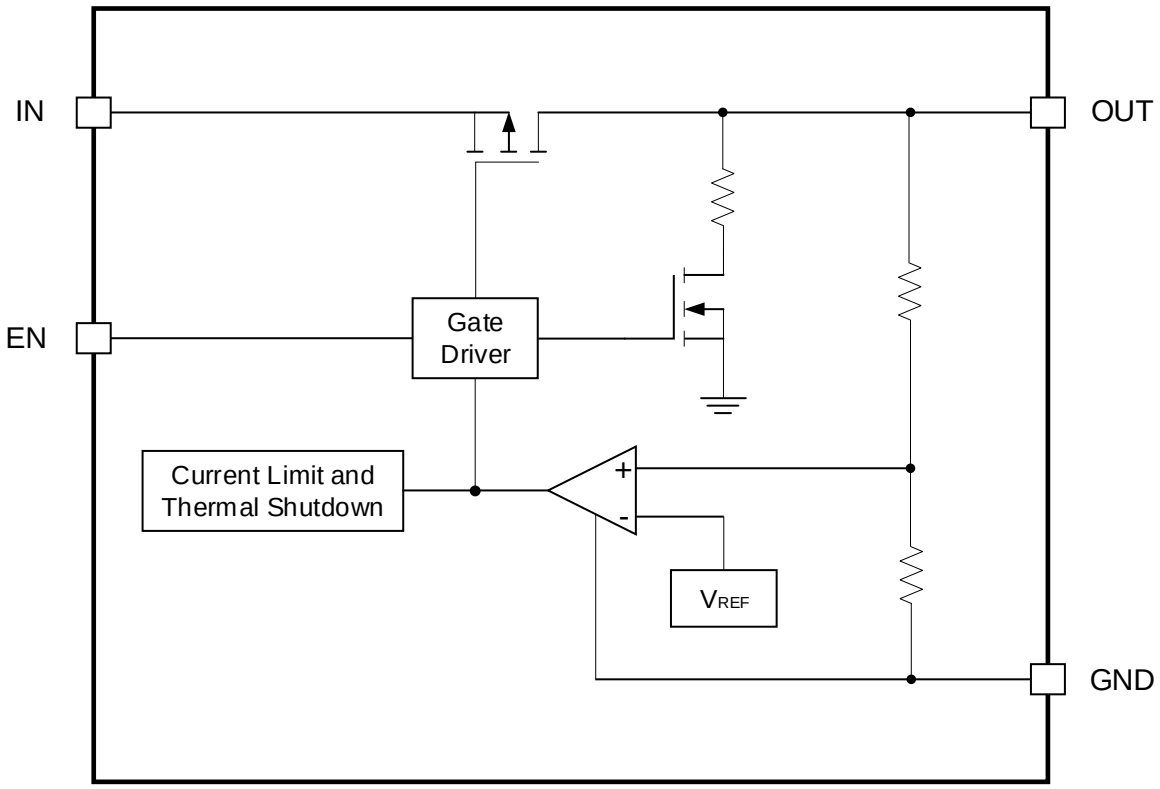


SOT89-3

PIN DESCRIPTIONS

Pin			Symbol	Description
DFN1.0 × 1.0-4	SOT23-5	SOT89-3		
1	5	3	OUT	Output pin. Bypass a 1 μF ceramic capacitor from this pin to ground.
2	2	1	GND	Ground.
3	3	/	EN	Enable control input, active high. Do not leave EN floating.
4	1	2	IN	Supply input pin. Must be closely decoupled to GND with a 1 μF or greater ceramic capacitor.
/	4	/	NC	No Connection.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Input Capacitor

A 1 μF ceramic capacitor is recommended to connect between IN and GND pins to decouple input power supply glitch and noise. The amount of the capacitance may be increased without limit. This input capacitor must be located as close as possible to the device to assure input stability and less noise. For PCB layout, a wide copper trace is required for both IN and GND. The input capacitor should be at least equal to, or greater than, the output capacitor for good load transient performance.

Output Capacitor

An output capacitor is required for the stability of the LDO. The recommended output capacitance is from 1 μF to 10 μF, Equivalent Series Resistance (ESR) is from 5 mΩ to 500 mΩ, and temperature characteristics are X7R or X5R. Higher capacitance values help to improve load/line transient response. The output capacitance may be increased to keep low undershoot/overshoot. Place output capacitor as close as possible to OUT and GND pins. With a reasonable PCB layout, the single 1 μF ceramic output capacitor can be placed up to 10 cm away from the SUM3452 device.

ON/OFF Input Operation

The SUM3452 EN pin is internally held low by a 1 MΩ resistor to GND. The SUM3452 is turned on by setting the EN pin higher than V_{IH} threshold, and is turned off by pulling it lower than V_{IL} threshold. If this feature is not used, the EN pin should be tied to IN pin to keep the regulator output on at all time.

High PSRR and Low Noise

RF circuits such as LNA (low-noise amplifier), up/down-converter, mixer, PLL, VCO, and IF stage, require low noise and high PSRR LDOs. The temperature-compensated crystal oscillator circuit requires very high PSRR at RF power amplifier burst frequency. For instance, minimum 65 dB PSRR at 217 Hz is recommended for the GSM handsets.

In order to provide good audio quality, the audio power supply for hand-free, game, MP3, and multimedia applications in cellular phones, require low-noise and high PSRR at audio frequency range (20 Hz - 20 kHz).

The SUM3452, with PSRR of 76 dB at 1 kHz, is suitable for most of these applications that require high PSRR and low noise.

Output Automatic Discharge

The SUM3452 output employs an internal 230 Ω (typical) pulldown resistance to discharge the output when the EN pin is low, and the device is disabled.

Remote Output Capacitor Placement

The SUM3452 requires at least a 1 μF capacitor at the OUT pin, but there are no strict requirements about the location of the capacitor in regards the OUT pin. In practical designs, the output capacitor may be located up to 10 cm away from the LDO.

Fast Transient Response

Fast transient response LDOs can also extend battery life. TDMA-based cell phone protocols such as Global System for Mobile Communications (GSM) have a transmit/receive duty factor of only 12.5 percent, enabling power savings by putting much of the baseband circuitry into standby mode in between transmit cycles. In baseband circuits, the load often transitions virtually instantaneously from 100 μA to 100 mA. To meet this load requirement, the LDO must react very quickly without a large voltage drop or overshoot — a requirement that cannot be met with conventional, general-purpose LDOs.

The SUM3452's fast transient response from 0 to 300 mA provides stable voltage supply for fast DSP and GSM chipset with fast changing load.

Low Quiescent Current

Cellular phone baseband internal digital circuits typically operate all the time. That requires LDO stays on at all times. However, in the standby mode, the microprocessor consumes only around 100 ~ 300 μA. Since the phone stays in standby for the longest percentage of time, using a 18 μA quiescent current LDO, instead of 100 μA, saves 88 μA and can substantially extends the battery standby time.

The SUM3452, consuming only 18 μA quiescent current, provides great power saving in portable and low power applications.

Minimum Operating Input Voltage (V_{IN})

The SUM3452 does not include any dedicated UVLO circuitry. The SUM3452 internal circuitry is not fully functional until V_{IN} is at least 1.8 V. The output voltage is not regulated until V_{IN} has reached at least the greater of 1.8 V or (V_{OUT} + V_{DROP}).

Current Limit Protection

When output current at the OUT pin is higher than current limit threshold or the OUT pin is short-circuit to GND, the current limit protection will be triggered and clamp the output current to approximately 500 mA to prevent over-current and to protect the regulator from damage due to overheating.

Thermal Overload Protection (TSD)

Thermal shutdown disables the output when the junction temperature rises to approximately 155°C which allows the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry enables. Based on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This thermal cycling limits the dissipation of the regulator and protects it from damage as a result of overheating.

The thermal shutdown circuitry of the SUM3452 has been designed to protect against temporary thermal overload conditions. The TSD circuitry was not intended to replace proper heat-sinking. Continuously running the SUM3452 device into thermal shutdown may degrade device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Rating	Unit
Operating Temperature Range	-40 to +85	℃

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min.	Max.	Unit
IN Voltage	V_{IN}	-0.3	6.0	V
Other Pin Voltage		-0.3	V_{IN} + 0.3	V
Maximum Load Current		Internal Limited		mA
Junction Temperature	T_J		+150	°C
Storage Temperature	T_{STG}	-65	+150	°C
Lead Temperature(Soldering, 10 sec)	T_L		300	°C

NOTE:

Stresses beyond those listed under "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. SUMSEMI recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

SUMSEMI reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time. Please contact SUMSEMI sales office to get the latest datasheet.

ELECTRICAL CHARACTERISTICS

T_A = +25°C, C_{IN} = 1 µF, C_{OUT} = 1 µF, unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IN}	Input Voltage Range		2.1		5.5	V
ΔV_{OUT}	Output Voltage Tolerance	V_{IN} = 2.8 V to 5.5 V, I_{OUT} = 1 mA to 300 mA	-2		2	$\%V_{OUT}$
	Line Regulation	V_{IN} = 2.8 V to 5.5 V, I_{OUT} = 1 mA		0.02		%mA
	Load Regulation	I_{OUT} = 1 mA to 300 mA		0.001		%mA
I_{LOAD}	Load Current			500		mA
I_{SHDN}	Input Shutdown Quiescent Current	Disabled, V_{EN} = 0 V,		0.2	1	µA
I_Q	Input Quiescent Current	V_{IN} > 2.1 V, V_{EN} > 1.2 V, I_{OUT} = 0 mA		18	25	µA
$I_{standby}$	Standby Current	V_{EN} = 0V		0.2	1	µA
V_{DROP}	Dropout Voltage	I_{OUT} = 100 mA		50		mV
		I_{OUT} = 300 mA		180		mV
		I_{OUT} = 500 mA		300		mV
I_{LMT}	Short Circuit Current Limit	T_A = 25°C		700		mA
PSRR	Power supply rejection ration	f = 100 Hz, I_{OUT} = 20 mA		80		dB
		f = 1 kHz, I_{OUT} = 20 mA		76		dB
		f = 10 kHz, I_{OUT} = 20 mA		65		dB
		f = 100 kHz, I_{OUT} = 20 mA		40		dB
e_N	Output Noise Voltage	BW = 10 Hz to 100 kHz, I_{OUT} = 1 mA		20		μV_{RMS}
		BW = 10 Hz to 100 kHz, I_{OUT} = 300 mA		6.5		μV_{RMS}
$R_{Dischrg}$	Output Discharge FET R_{DSON}	V_{EN} < V_{IL} (output disable)	20	30	40	Ω
V_{IL}	EN Input Logic Low Voltage	V_{IN} = 1.8 V to 5.5 V, V_{EN} falling until the output is disabled			0.4	V
V_{IH}	EN Input Logic High Voltage	V_{IN} = 1.8 V to 5.5 V, V_{EN} rising until the output is enabled	1			V
I_{EN}	EN Input leakage current	V_{IN} = 5.5 V ,V_{EN} = 0 V		0.01	1	µA
		V_{IN} = 5.5 V ,V_{EN} = 5.5 V		5.5		µA
T_{SHDN}	Thermal shutdown threshold	V_{IN} = 2.8 V, T_J rising		155		°C
T_{HYS}	Thermal shutdown hysteresis	V_{IN} = 2.8 V, T_J falling from shutdown		15		°C

Note:

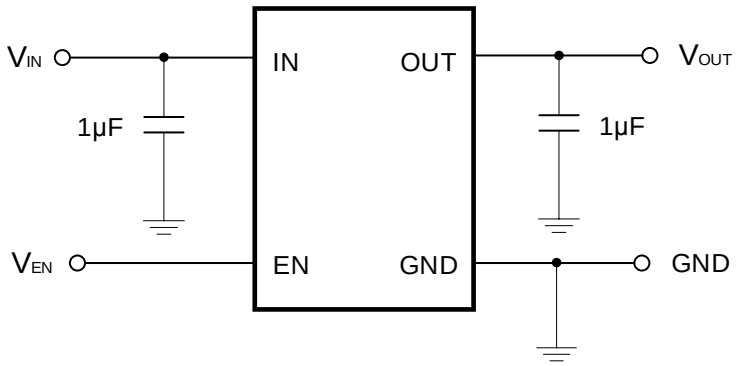
(1) V_{DROP} is measured for devices with V_{OUT} ≥ 1.5 V.

ELECTRICAL CHARACTERISTICS (Continued)

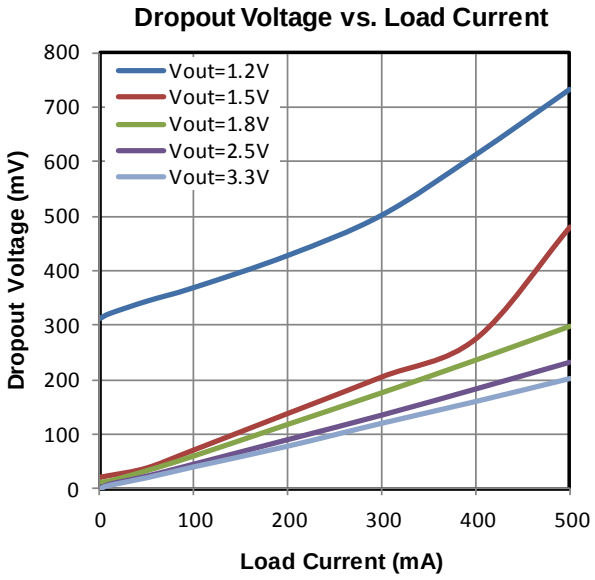
T_A = +25°C, C_{IN} = 1 µF, C_{OUT} = 1 µF, unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
ΔV_{OUT}	Line transient	V_{IN} = ($V_{OUT(NOM)}$ + 1 V) to ($V_{OUT(NOM)}$ + 1.6 V) in 10 µs		10		mV
		V_{IN} = ($V_{OUT(NOM)}$ + 1.6 V) to ($V_{OUT(NOM)}$ + 1 V) in 10 µs		10		mV
	Load transient	I_{OUT} = 1 mA to 300 mA in 10 µs		20		mV
		I_{OUT} = 300 mA to 1 mA in 10 µs		20		mV
Overshoot	Overshoot on start-up	Stated as percentage of $V_{OUT(NOM)}$			5	%
$T_{D(ON)}$	Output Turn-on Delay Time	From V_{EN} > V_{IH} to V_{OUT} = 95% of $V_{OUT(NOM)}$		150	250	µs

APPLICATION CIRCUITS

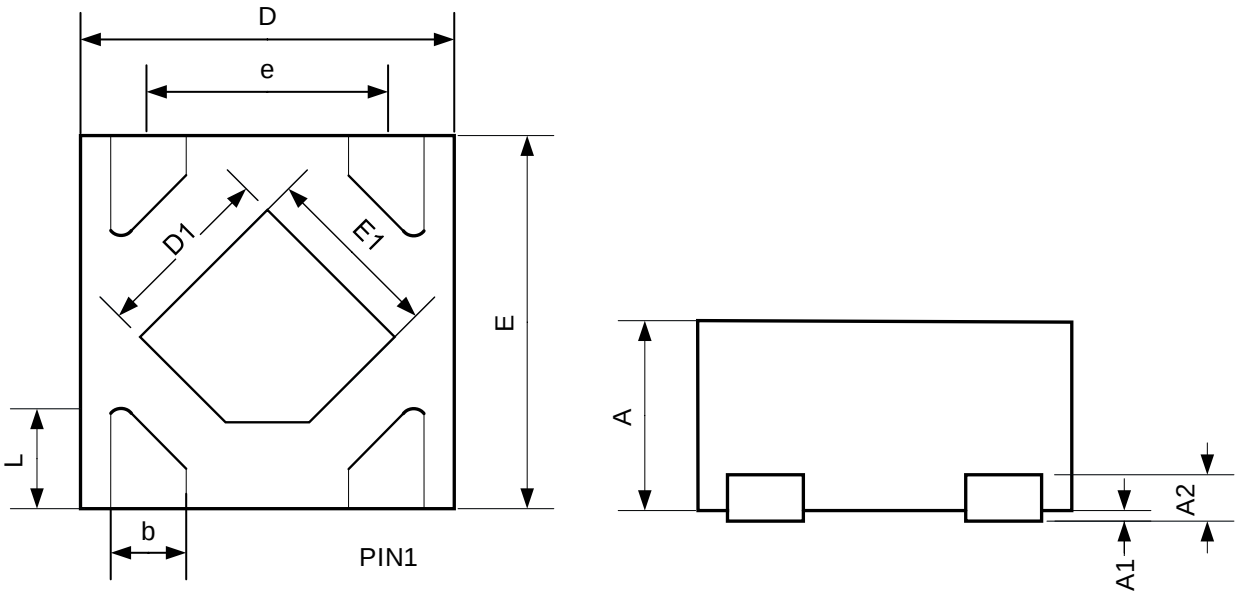


TYPICAL PERFORMANCE CHARACTERISTICS



PACKAGE OUTLINE

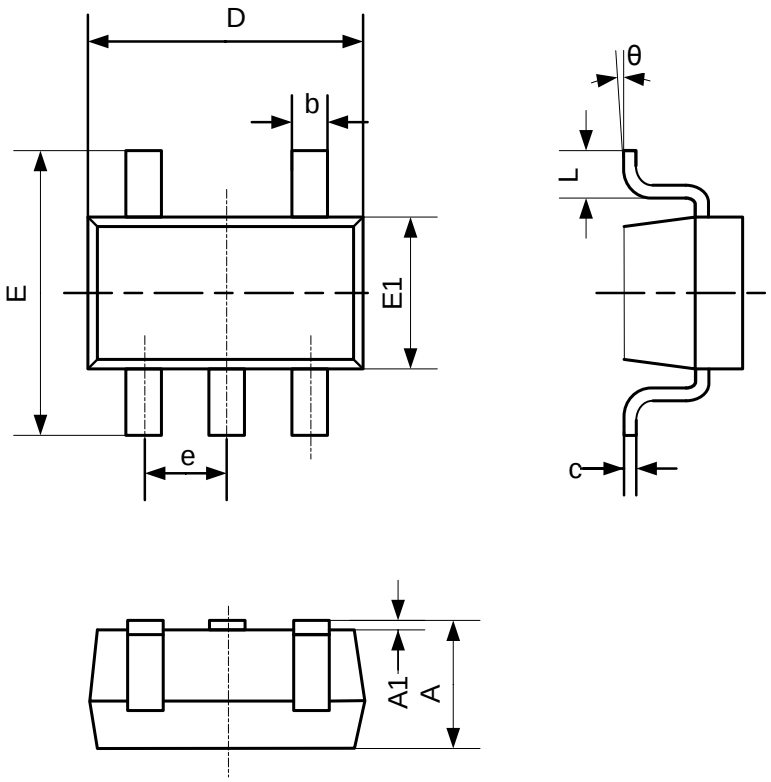
DFN1.0 × 1.0-4



Symbol	Dimensions In Millimeters	
	Min	Max
A	0.400	0.550
A1	0.000	0.050
A2	0.125REF	
b	0.150	0.250
D	0.950	1.050
D1	0.380	0.580
E	0.950	1.050
E1	0.380	0.580
e	0.650BSC	
L	0.150	0.350

PACKAGE OUTLINE

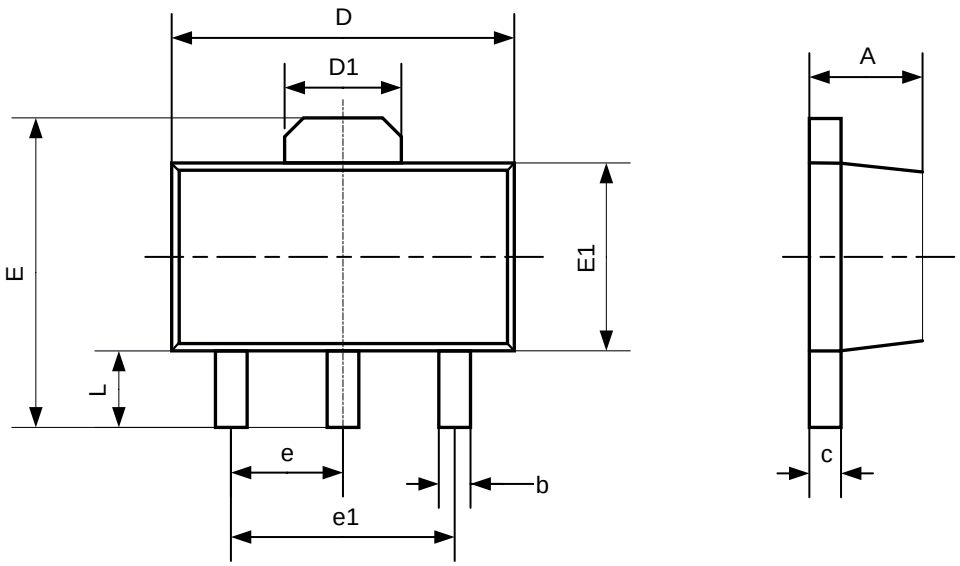
SOT23-5



Symbol	Dimensions In Millimeters	
	Min	Max
A	0.700	1.250
A1	0.000	0.100
b	0.300	0.500
c	0.100	0.200
D	2.820	3.020
E	2.650	2.950
E1	1.500	1.700
e	0.950BSC	
L	0.300	0.600
θ	0°	8°

PACKAGE OUTLINE

SOT89-3



Symbol	Dimensions In Millimeters	
	Min	Max
A	1.400	1.600
b	0.320	0.520
c	0.350	0.440
D	4.400	4.600
D1	1.550REF	
E	3.940	4.250
E1	2.300	2.600
e	1.500BSC	
e1	3.000BSC	
L	0.900	1.200

V 1.5