High PSRR Low Noise 600mA LDO

GENERAL DESCRIPTION

The SUM3473 family of low-dropout (LDO), low-power linear regulators offers high power supply rejection ratio (PSRR) while maintaining low 50 µA ground current, suitable for RF applications. The family uses an advanced CMOS process and a PMOSFET pass device to achieve fast start-up, low noise, excellent transient response, and excellent PSRR performance. The SUM3473 is stable with a 1.0 µF ceramic output capacitor, and uses a precision voltage reference and feedback loop to achieve a worst-case accuracy of 2% over all load, line, process, and temperature variations. It is fully specified from T_J = –40°C to +150°C and is offered in DFN1.0 × 1.0-4 and SOT23-5 packages, which is ideal for small form factor portable equipment such as wireless handsets and PDAs.

FEATURES

- Wide Input Voltage Range: 2.0 V to 6.0 V
- Up to 600mA Load Current
- Standard Fixed Output Voltage Options: 1.2 V, 1.8 V, 3.0 V, 3.3 V
- Other Output Voltage Options Available on Request
- Low I_Q: 50 µA
- Low Dropout: 250mV at 400 mA Load@V_{OUT}=3.3 V
- High PSRR: 60 dB at 1KHz
- Low Noise: 60 µVrms at 1.8 V output
- Fast Start-Up Time: 25 µs
- Excellent Load/Line Transient Response
- Line Regulation: 0.03% typical
- Package: DFN1.0 × 1.0-4, SOT23-5

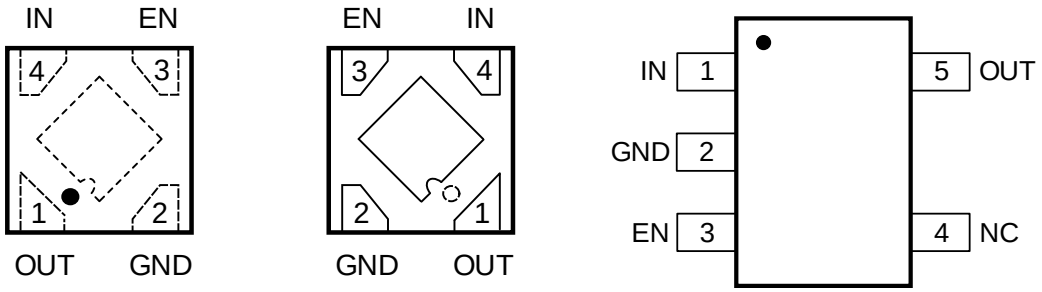
APPLICATIONS

- Smart Phones and Cellular Phones
- PDAs
- MP3/MP4 Player
- Digital Still Cameras
- Portable instruments

ORDER INFORMATION

Model	Package	Ordering Number	Packing Option
SUM3473	DFN1.0 × 1.0-4	SUM3473-XXYB	Tape and Reel, 10000
	SOT23-5	SUM3473-XXKA5	Tape and Reel, 3000

PIN CONFIGURATION

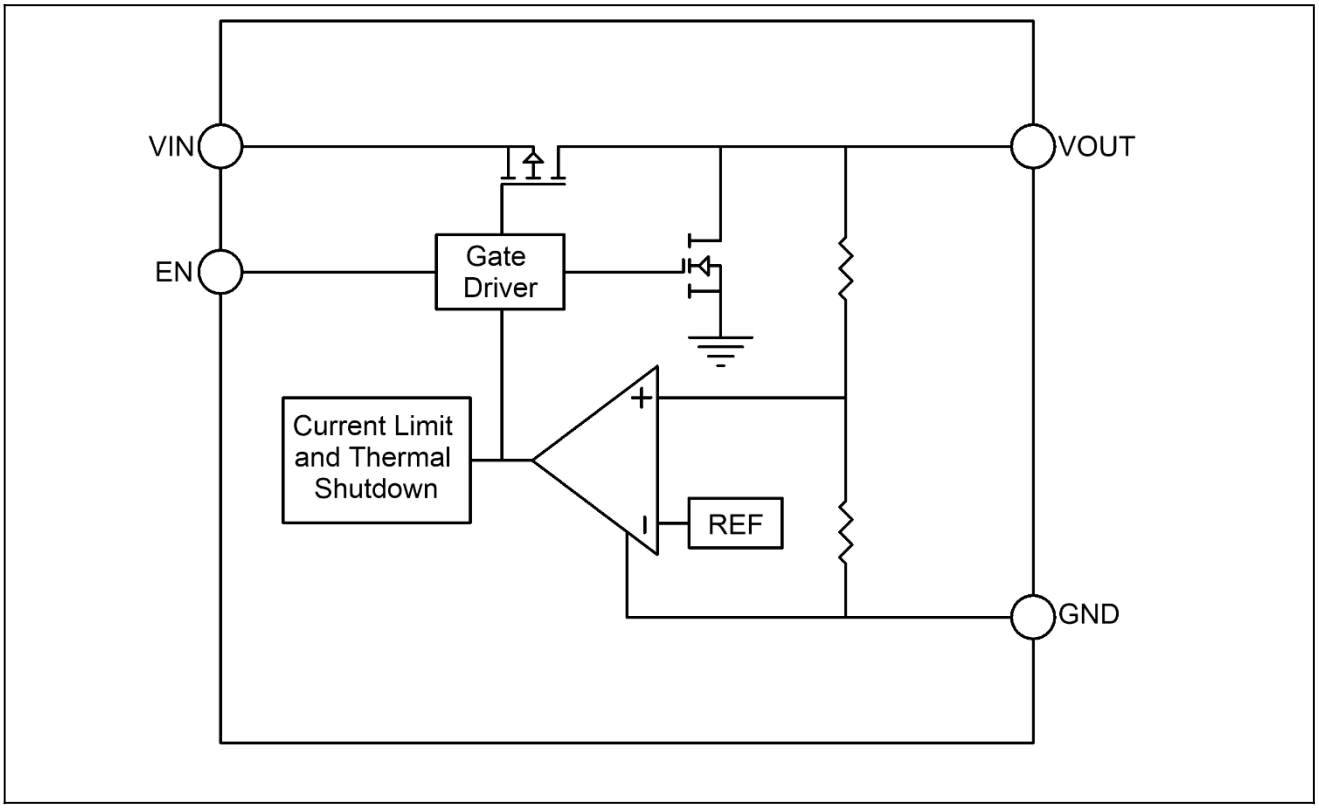


DFN1.0 × 1.0-4 SOT23-5

PIN FUNCTION

Pin Number		Pin Name	Function
DFN1.0×1.0-4	SOT23-5		
1	5	OUT	Output pin. Bypass a 1 μF ceramic capacitor from this pin to ground.
2	2	GND	Ground.
3	3	EN	Enable control input, active high. Do not leave EN floating.
	4	NC	No connection.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Input Capacitor

A 1 μF ceramic capacitor is recommended to connect between V_{IN} and GND pins to decouple input power supply glitch and noise. The amount of the capacitance may be increased without limit. This input capacitor must be located as close as possible to the device to assure input stability and less noise. For PCB layout, a wide copper trace is required for both V_{IN} and GND.

Output Capacitor

An output capacitor is required for the stability of the LDO. The recommended output capacitance is from 1 μF to 2.2 μF, Equivalent Series Resistance (ESR) is from 5 mΩ to 100 mΩ, and temperature characteristics are X7R or X5R. Higher capacitance values help to improve load/line transient response. The output capacitance may be increased to keep low undershoot/overshoot. Place output capacitor as close as possible to OUT and GND pins.

ON/OFF Input Operation

The SUM3473 is turned on by setting the EN pin high, and is turned off by pulling it low. If this feature is not used, the EN pin should be tied to IN pin to keep the regulator output on at all time.

High PSRR and Low Noise

RF circuits such as LNA (low-noise amplifier), up/down-converter, mixer, PLL, VCO, and IF stage, require low noise and high PSRR LDOs. The temperature-compensated crystal oscillator circuit requires high PSRR

at RF power amplifier burst frequency. For instance, minimum 60 dB PSRR at 217 Hz is recommended for the GSM handsets.

The SUM3473, with PSRR of 60 dB at 1 KHz, is suitable for most of these applications that require high PSRR and low noise.

Ultra Fast Start-up

After enabled, the SUM3473 is able to provide full power in as little as tens of microseconds, typically 25 μs. This feature will help load circuitry move in and out of standby mode in real time, eventually extend battery life for mobile phones and other portable devices.

Fast Transient Response

Fast transient response LDOs can also extend battery life. To meet this load requirement, the LDO must react very quickly without a large voltage drop or overshoot — a requirement that cannot be met with conventional, general-purpose LDOs.

The SUM3473's fast transient response from 0 to 150 mA provides stable voltage supply for fast DSP and GSM chipset with fast changing load.

Low Quiescent Current

The SUM3473, consuming only around 40 μA for all input range and output loading, provides great power saving in portable and low power applications.

Current Limit Protection

When output current at the OUT pin is higher than current limit threshold or the OUT pin is short-circuit to GND, the current limit protection will be triggered and clamp the output current to approximately 650 mA to prevent over-current and to protect the regulator from damage due to overheating.

Thermal Shutdown Protection

Thermal protection disables the output when the junction temperature rises to approximately +155°C, allowing the device to cool down. When the junction temperature reduces to approximately +130°C the output circuitry is enabled again. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the heat dissipation of the regulator, protecting it from damage due to overheating.

RECOMMENDED OPERATING CONDITIONS

Symbol	Item	Rating	Unit
V_{IN}	Input Voltage	2.0 to 6.0	V
I_{OUT}	Output Current	0 to 600	mA
T_A	Operating Ambient Temperature	-40 to 85	°C
C_{IN}	Effective Input Ceramic Capacitor Value	0.47 to 4.7	uF
C_{OUT}	Effective Output Ceramic Capacitor Value	0.47 to 4.7	uF
ESR	Input and Output Capacitor Equivalent Series Resistance	5 to 100	mΩ

ABSOLUTE MAXIMUM RATINGS(2)

Parameter	Rating		Unit
IN Voltage	-0.3 to 6.5		V
Other Pin Voltage	-0.3 to V_{IN}+0.3		V
Maximum Load Current	650		mA
Junction to Ambient Thermal Resistance (θ_{JA}),(1)	DFN1.0 × 1.0-4	280	°C/W
	SOT23-5	250	
Operating Junction Temperature	-40 to 150		°C
Storage Temperature	-65 to 150		°C
Lead Temperature (Soldering, 10 sec)	300		°C

NOTE:

(1) This particular frame decreases the total thermal resistance of the package and increases its ability to dissipate power when an appropriate area of copper on the printed circuit board is available for heat-sinking.

(2) Stresses beyond those listed under “ABSOLUTE MAXIMUM RATINGS” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

This integrated circuit can be damaged by ESD if you don’t pay attention to ESD protection. SUMSEMI recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

SUMSEMI reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time. Please contact SUMSEMI sales office to get the latest datasheet.

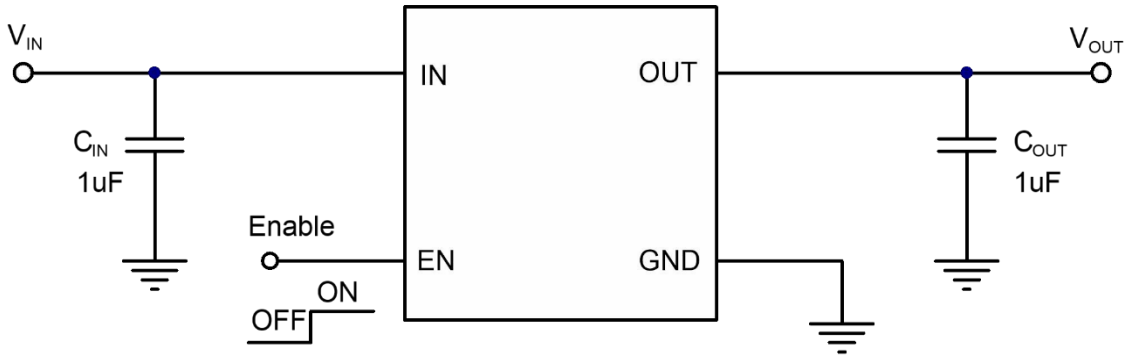
ELECTRICAL CHARACTERISTICS

(V_{IN}=V_{EN}=V_{OUT} + 1.0 V, I_{OUT}= 1 mA, C_{IN}= 1μF, C_{OUT}=1μF, Typical values are at T_A=25°C unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Operation Range	V_{IN}		2.0		6.0	V
Dropout Voltage	V_{DROP}	V_{OUT} = 1.8V, I_{OUT} = 400mA		320	400	mV
		V_{OUT} = 3.3V, I_{OUT} = 400mA		185	330	
DC Supply Quiescent Current	I_{Q_ON}	Active mode: V_{EN}=V_{IN}		50	70	μA
DC Supply Shutdown Current	$I_{Q\ OFF}$	V_{EN}=0V		0.01	1	μA
Regulated Output Voltage	V_{OUT}	I_{OUT}=1mA, -40°C≤T_A≤85°C	-2		2	%
Output Voltage Line Regulation	Reg_{LINE}	V_{IN} = V_{OUT} +1V to 5.5V, I_{OUT} = 10mA		0.03	0.2	%
Output Voltage Load Regulation	Reg_{LOAD}	I_{OUT} from 1mA to 300mA		20	40	mV
Current Limit	I_{LIM}		600			mA
Power Supply Rejection Ratio	PSRR	f=1kHz, C_{OUT}=1μF, I_{OUT}=20mA		60		dB
		f=10kHz, C_{OUT}=1μF, I_{OUT}=20mA		58		
Output Noise	e_N	10Hz to 100kHz, I_{OUT} =100mA, C_{OUT} = 1μF		60		$μV_{RMS}$
Soft-start Time	T_{ON}	From Enable to Power On		25		μs
EN Low Threshold	V_{ENL}				0.4	V
EN High Threshold	V_{ENH}		1.0			V
EN pull-down resistance	R_{PD}		0.8	1	1.3	MΩ
Over-temperature Shutdown Threshold	T_{TSD}			155		°C
Over-temperature Shutdown Hysteresis	T_{TSR}			20		°C

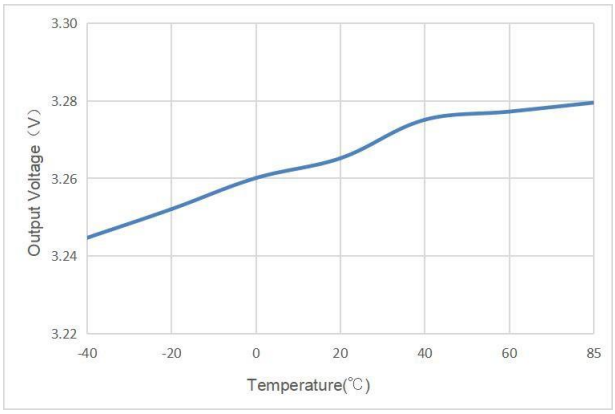
Note:Test at+25°C.Specifications over the temperature range are guaranteed by design and characterization.

APPLICATION CIRCUITS

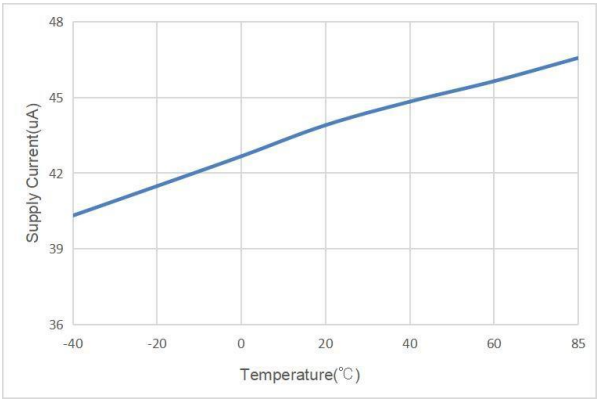


TYPICAL CHARACTERISTICS

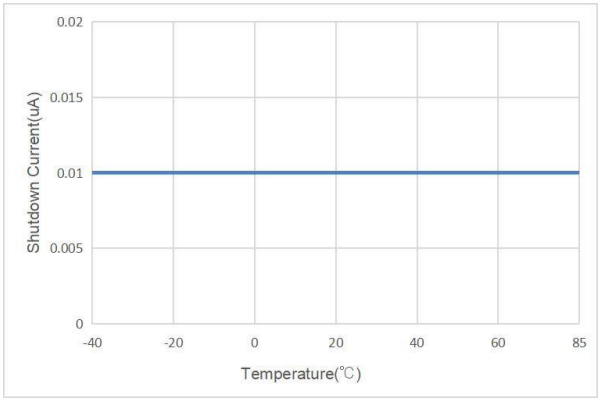
(V_{OUT}= 3.3V, V_{IN} = 4.3V, I_{OUT} = 1mA ,C_{IN} = Ceramic 1.0μF, C_{OUT} = Ceramic 1.0μF,T_A= -40°C~85°C)



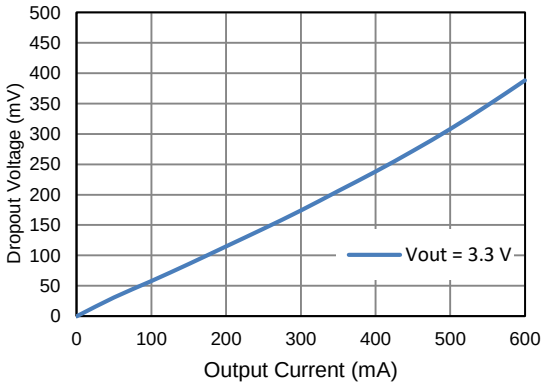
Output Voltage VS Temperature



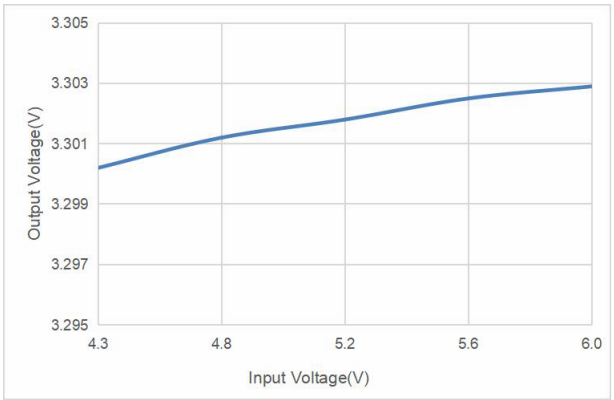
Supply Current VS Temperature



Shutdown Current VS Temperature



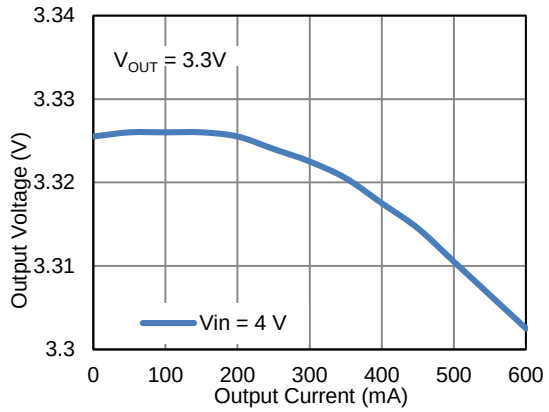
Dropout Voltage VS Output Current



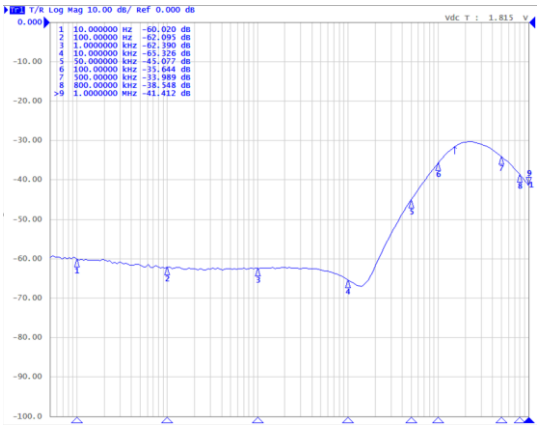
Output Voltage VS V_{IN} Input Voltage

TYPICAL CHARACTERISTICS(CONTINUED)

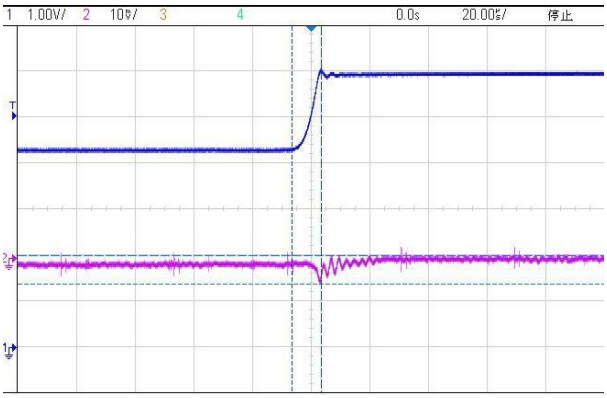
(V_{OUT} = 3.3 V, V_{IN} = 4.3 V, I_{OUT} = 1 mA ,C_{IN} = Ceramic 1.0 μF, C_{OUT} = Ceramic 1.0 μF,T_A=-40°C~85°C)



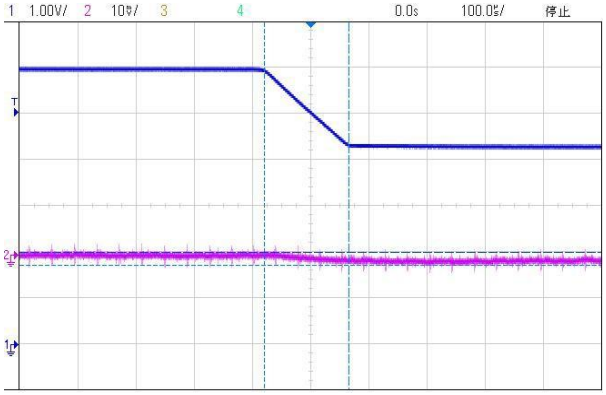
Output Voltage VS Output Current



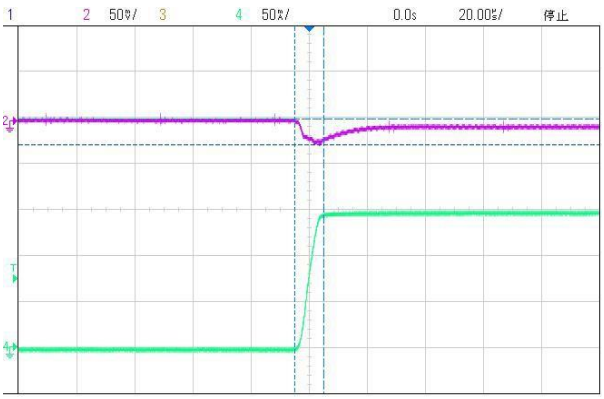
PSRR



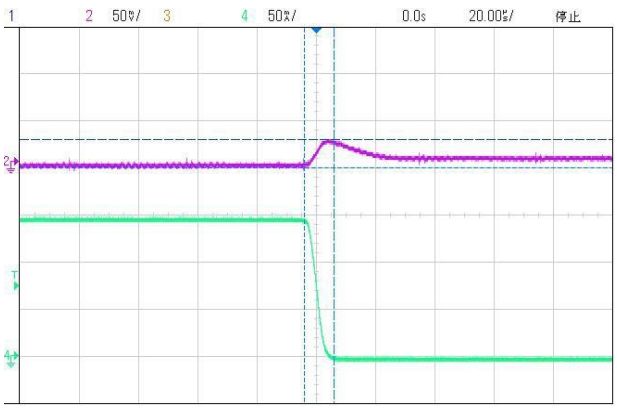
Input Transient(4.3~6V t=10us 10mA)



Input Transient(6~4.3V t=10us 10mA)



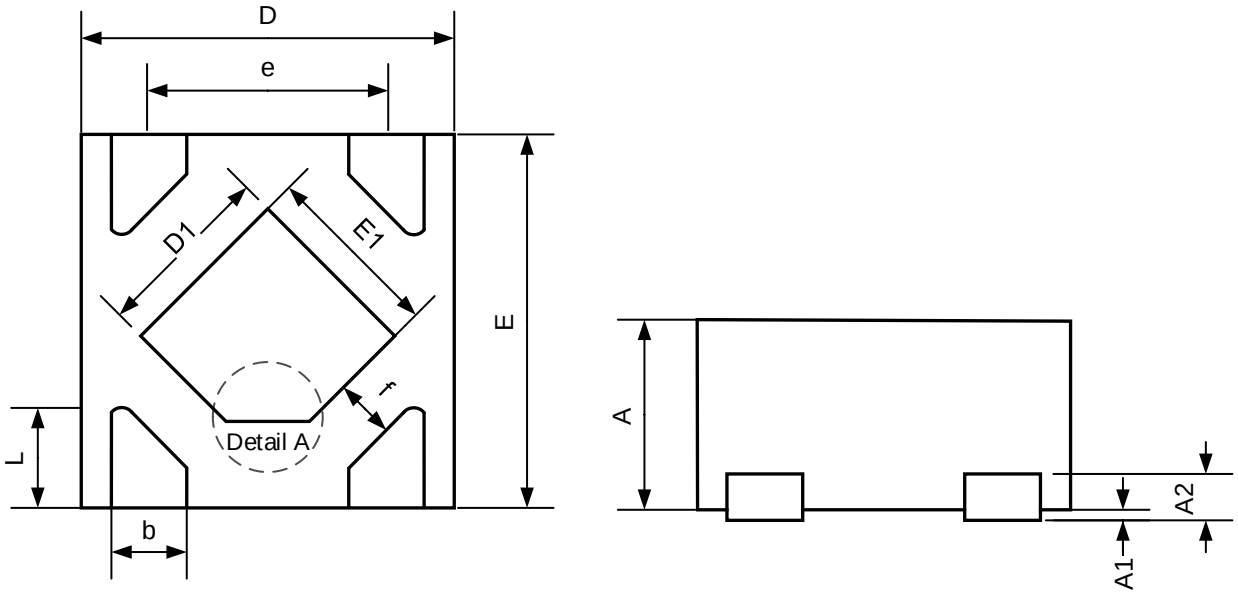
Load Transient(1mA~150mA t=10us)



Load Transient(150mA~1mA t=10us)

PACKAGE DIMENSION

DFN1.0 × 1.0-4



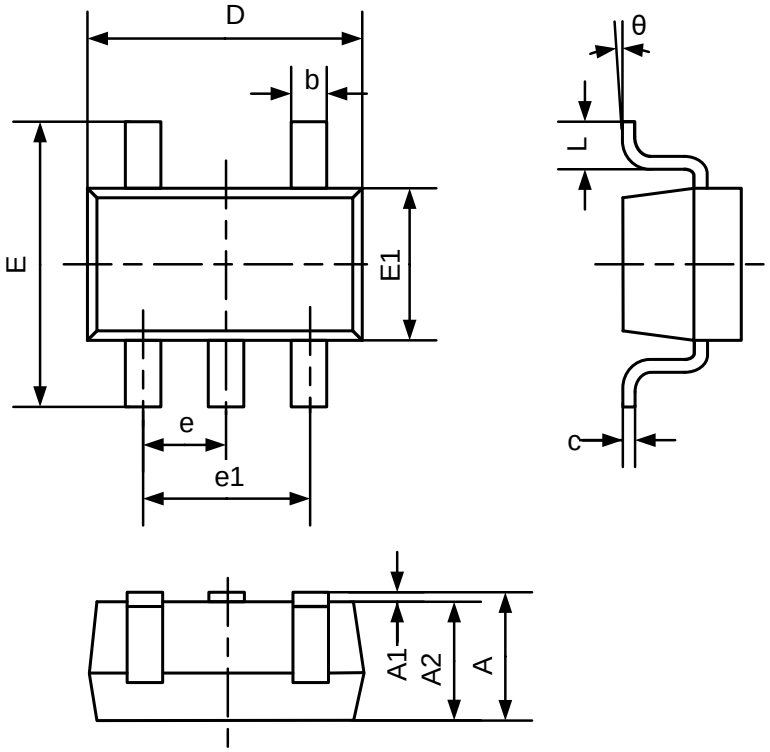
Detail A:

Note: Detail A has two kinds of shapes

Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	0.400	0.500	0.550
A1	0.000	0.025	0.050
A2		0.125REF	
D	0.950	1.000	1.050
D1	0.380	0.480	0.580
E	0.950	1.000	1.050
E1	0.380	0.480	0.580
b	0.150	0.200	0.250
e		0.650BSC	
f	0.190	0.195	0.200
L	0.150	0.250	0.350

PACKAGE DIMENSION

SOT23-5



Symbol	Dimensions In Millimeters	
	MIN	MAX
A	0.700	1.250
A1	0.000	0.100
A2	0.700	1.150
b	0.350	0.500
c	0.080	0.200
D	2.820	3.020
E	2.650	2.950
E1	1.500	1.700
e	0.950BSC	
e1	1.800	2.000
L	0.300	0.600
θ	0°	8°

V 1.3