20V 1A High Speed LDO Regulator

DESCRIPTION

The SUM3563 is low noise, LDO Voltage Regulators with enable function that output voltages of 3.3 V, 5.0 V. These characteristics, combined with low noise and good PSRR with low dropout voltage, make this device ideal for portable consumer applications.

The SUM3563 can operate with up to 20 V input. The Devices are available in SOT-223, SOT89-3, DFN2 × 2-6, DFN3 × 3-8 and ESOP-8.

FEATURES

- Operating Input Voltage Range: up to 20 V
- Max Output Current: 1 A
- Output Voltage Accuracy: ±2%
- Adjustable Output Voltage Option V_{FB} = 0.64 V
- Standard Fixed Output Voltage Options: 3.3 V, 5.0 V
- Other Output Voltage Options Available on Request
- Standby Current: 160 μA (Typical)
- High Ripple Rejection: 80 dB at 1 kHz
- Packages: SOT-223, SOT89-3, DFN2 × 2-6, DFN3 × 3-8 and ESOP-8
- Dropout: 0.5 V at 1 A when V_{OUT} ≥ 2 V

APPLICATIONS

- Consumer and Industrial Equipment Point of Regulation.
- Switching Power Supply Post Regulation
- Battery Chargers
- Hard Drive Controllers

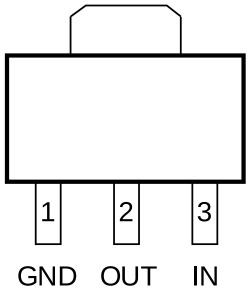
ORDER INFORMATION

Model	Package	Ordering Number	Packing Option
SUM3563	SOT-223	SUM3563-XXKD	Tape and Reel, 2500
	SOT89-3	SUM3563-XXP	Tape and Reel, 1000
	DFN2 × 2-6	SUM3563-ADJDNE6	Tape and Reel, 3000
	DFN3 × 3-8	SUM3563-ADJDNB8	Tape and Reel, 4000
	ESOP-8	SUM3563-ADJES8	Tape and Reel, 4000

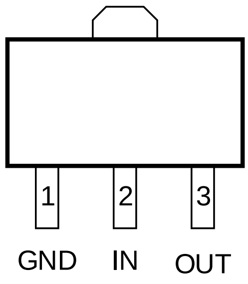
*XX: When expressed as 33, the output voltage is 3.3 V; when expressed as 50 the output voltage is 5.0 V;

ADJ: Adjustable Output Voltage, Rang: 0.6 V to 5.5 V.

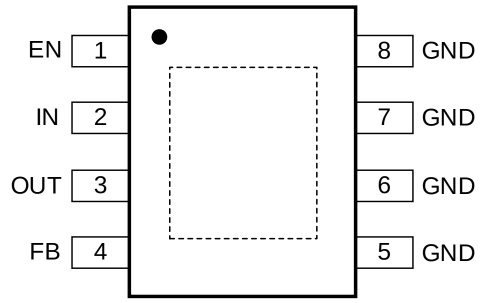
PIN CONFIGURATION (Top View)



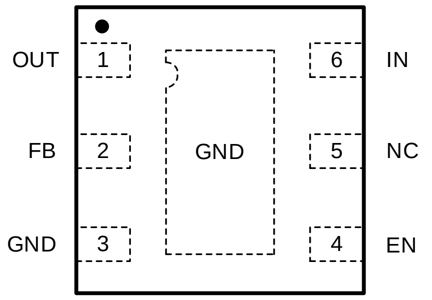
SOT-223



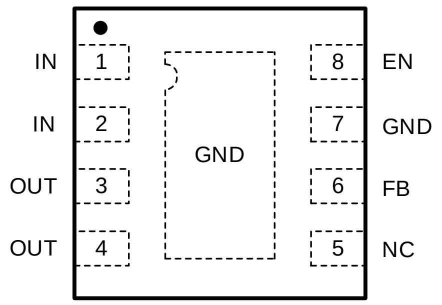
SOT89-3



ESOP-8



DFN2 × 2-6

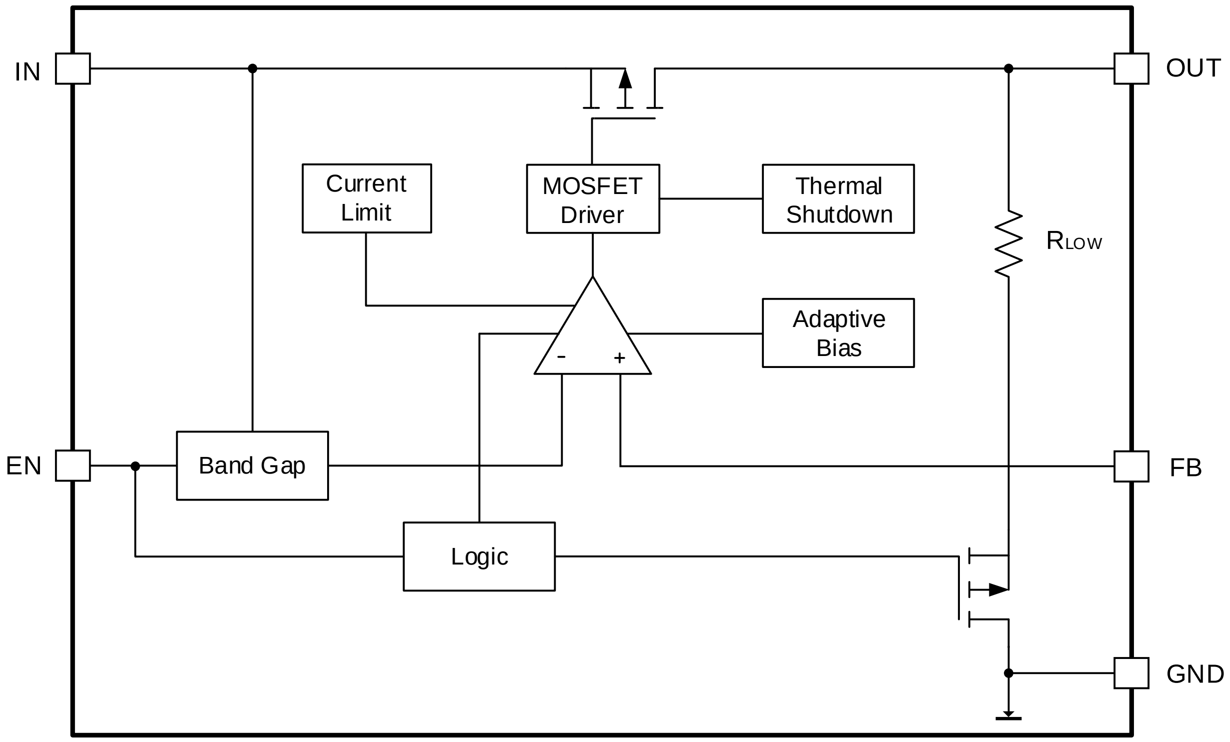


DFN3 × 3-8

PIN DESCRIPTIONS

Pin					**Symbol**	**Description**
SOT-223	SOT89-3	ESOP-8	DFN2 × 2-6	DFN3 × 3-8		
1	1	5,6,7,8	3	7	GND	Ground.
2	3	3	1	3,4	OUT	Output pin.
3	2	2	6	1,2	IN	Power supply input pin.
		1	4	8	EN	Enable pin.
		4	2	6	FB	This pin is used as an input to the control loop error amplifier and is used to set the output voltage of the LDO.
			5	5	NC	Not connect.
		Exposed Pad	Exposed Pad	Exposed Pad	GND	Exposed thermal pad. Connect to GND for best thermal performance.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Enable

The SUM3563 delivers the output power when it is set to enable state. When it works in disable state, there is no output power and the operation quiescent current is almost zero. The enable pin (EN) is active high.

Shutdown

Turn off the device by forcing the EN pin to drop below $V_{EN(LO)}$. If shutdown capability is not required, connect EN to IN. The SUM3563 has an internal pulldown MOSFET that connects an $R_{PULLDOWN}$ resistor to ground when the device is disabled. The discharge time after disabling depends on the output capacitance (C_{OUT}) and the load resistance (R_L) in parallel with the pulldown resistor ($R_{PULLDOWN}$). Formula 1 calculates the time constant:

$$\tau = (R_{PULLDOWN} \times R_L) / (R_{PULLDOWN} + R_L) \quad (1)$$

Over-Temperature Protection

The over-temperature protection function will turn off the P-MOSFET when the junction temperature exceeds 150°C (typical). Once the junction temperature cools down by approximately 20°C the regulator will automatically resume operation.

Current-Limit Protection

The SUM3563 provides current limit function to prevent the device from damages during over-load or shorted-circuit condition. This current is detected by an internal sensing transistor.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Rating	Unit
Input Voltage	V_{IN}	up to 20	V
Output Current	I_{OUT}	0 to 1	A
Operating Ambient Temperature	T_A	-40 to 85	℃
Effective Input Ceramic Capacitor Value(1)	C_{IN}	1 to 10	μF
Effective Output Ceramic Capacitor Value(1)	C_{OUT}	1 to 10	μF
Input and Output Capacitor Equivalent Series Resistance (ESR)	ESR	5 to 100	mΩ

(1) The capacitor is a chip capacitor, and larger capacitance value is required if electrolytic capacitor is used.

ABSOLUTE MAXIMUM RATINGS

Parameter		Rating		Unit
Input Voltage(1)		24		V
Output Voltage		0.65 to 6		V
Chip Enable Input		-0.3 to 22		V
Maximum Junction Temperature		150		℃
Storage Temperature		-65 to 150		℃
ESD	HBM(2)	2000		V
	CDM(2)	1500		V
Current Maximum Rating(3)		200		mA
Thermal Characteristics, Thermal Resistance, Junction-to-Air (4)		SOT-223	80	°C/W
		SOT89-3	120	°C/W
		DFN2 × 2-6	105	°C/W
		DFN3 × 3-8	65	°C/W
		ESOP-8	60	°C/W

NOTES:

Stresses beyond those listed under "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(1) Refer to ELECTRICAL CHARACTERISTIS and APPLICATION INFORMATION for Safe Operating Area.

(2) This device series incorporates ESD protection and is tested by the following methods:
ESD Human Body Model tested per EIA/JESD22-A114
CDM tested per JESD22-C101

(3) Latch up Current Maximum Rating tested per JEDEC78

(4) This particular frame decreases the total thermal resistance of the package and increases its ability to dissipate power when an appropriate area of copper on the printed circuit board is available for heat-sinking.

CAUTION

This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. SUMSEMI recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications. SUMSEMI reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time. Please contact SUMSEMI sales office to get the latest datasheet.

ELECTRICAL CHARACTERISTICS

$V_{IN} = V_{OUT} + 1$ V; $I_{OUT} = 10$ mA, $C_{IN} = C_{OUT} = 1.0$ μF, unless otherwise noted. Typical values are at $T_A = +25°C$.(1)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Operating Input Voltage	V_{IN}					20	V
Output Voltage	V_{OUT}	$T_A = +25°C$		-2%		+2%	V
		$-40°C \le T_A \le 85°C$		-3%		+3%	
Reference Voltage	V_{FB}	$T_A = +25°C$			0.64		V
Line Regulation	Reg_{LINE}	$2.5\ V \le V_{IN} \le 20$ V, $I_{OUT} = 10$ mA			0.05	0.20	%/V
Dropout Voltage	V_{DROP}	$-40°C \le T_A \le 125°C$, $V_{IN} \ge 2.5$ V, $I_{OUT} = 1$ A	$0.65\ V \le V_{OUT} < 1$ V			2500	mV
			$1\ V \le V_{OUT} < 1.5$ V			2000	
			$1.5\ V \le V_{OUT} < 2$ V			1000	
			$2\ V \le V_{OUT} < 2.5$ V			800	
			$2.5V \le V_{OUT} < 5.5$ V		450	598	
Load Regulation	Reg_{LOAD}	$1\ mA \le I_{OUT} \le 800$ mA, $V_{IN} = V_{OUT} + 1$ V				40	mV
Current Limit	I_{LMT}	$V_{IN} = V_{OUT} + 1$ V		1.04	1.3		A
Short Circuit Current Limit	I_{SHORT}	$V_{OUT} = 0$ V		350			mA
Quiescent Current	I_Q	$I_{OUT} = 0$ mA, (R1+R2) > 100 kΩ			160	190	μA
Standby Current	I_{Q_OFF}	$V_{EN} = 0$ V, $T_A = 25°C$			0.1	1	μA
EN Pin Threshold Voltage	V_{ENH}	EN Input Voltage "H"		1.2			V
EN Pin Threshold Voltage	V_{ENL}	EN Input Voltage "L"				0.4	V
EN Pin Current	I_{EN}	$V_{EN} \le V_{IN} \le 20$ V			1		μA
Power Supply Rejection Ratio	PSRR	$V_{IN} = V_{OUT} + 1$ V, $I_{OUT} = 50$ mA,	f = 1 kHz		80		dB
			f = 100 kHz		70		
			f = 1M kHz		65		
Output Noise Voltage	e_N	$V_{IN} = V_{OUT} + 1$ V, $I_{OUT} = 1$ mA, f = 10 Hz to 100 kHz, $V_{OUT} = 3$ V, $C_{OUT} = 1$ μF(2)			60		$μV_{RMS}$
Active Output Discharge Resistance (A option only)	R_{LOW}	$V_{IN} = 4$ V, $V_{EN} = 0$ V			70		Ω
Thermal Shutdown Temperature	T_{SD}	Temperature Increasing from $T_A = +25°C$(2)			150		℃
Thermal Shutdown Hysteresis	T_{SDH}	Temperature Falling from TSD(2)			25		℃

(1) Here V_{IN} means internal circuit can work normal. If $V_{IN} < V_{OUT}$, Output voltage follow V_{IN} ($I_{OUT} = 1$ mA),circuit is safety.

(2) Guaranteed by design and characterization. not a FT item.

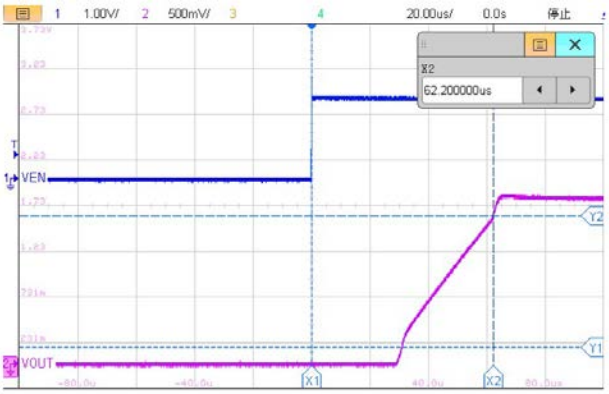
(3) V_{DROP} FT test method: test the V_{OUT} voltage at $V_{SET} + V_{DROP(MAX)}$ with 1 A output current.

(4) The minimum operating voltage is 2.5 V. $V_{DROP} = V_{IN(MIN)} - V_{OUT}$.

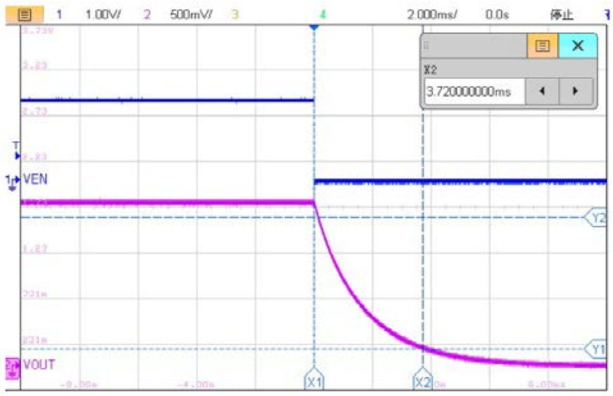
TYPICAL PERFORMANCE CHARACTERISTICS

Note: Typical Characteristics are intended to be used as reference data; they are not guaranteed.
($V_{IN} = V_{OUT} + 1$ V, I_{OUT} = 1 mA, C_{IN} = Ceramic 10 μF, C_{OUT} = Ceramic 10 μF)

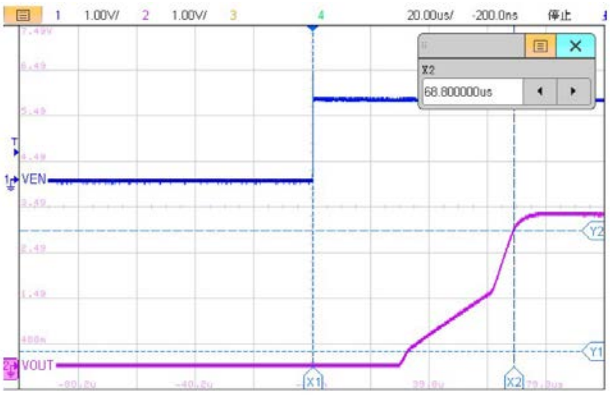
T_{ON} and T_{OFF}



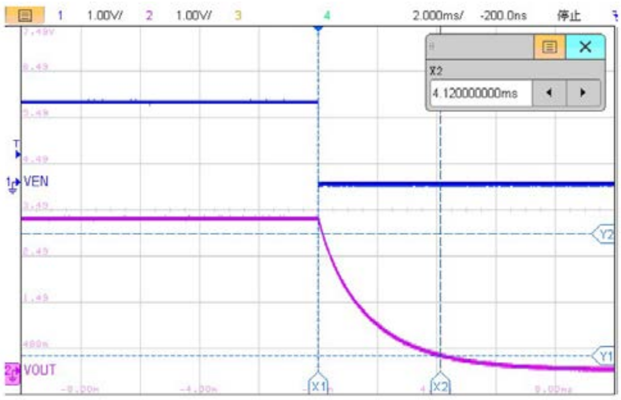
Turn On VS. EN Voltage (V_{OUT} = 1.8 V, I_{OUT} = 0 mA)



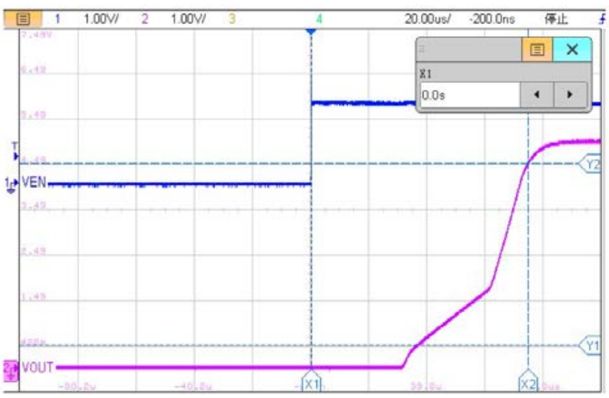
Turn Off VS. EN Voltage (V_{OUT} = 1.8 V, I_{OUT} = 0 mA)



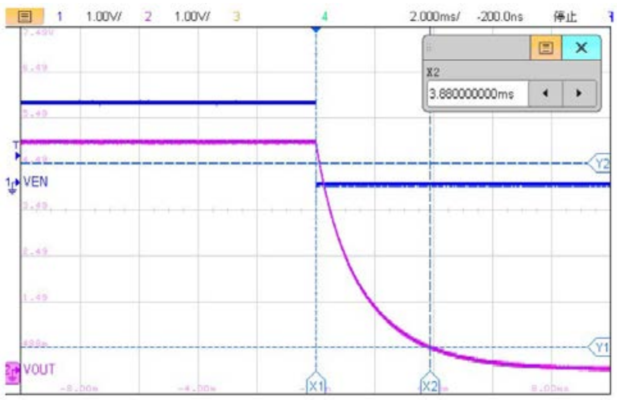
Turn On VS. EN Voltage (V_{OUT} = 3.3 V, I_{OUT} = 0 mA)



Turn Off VS. EN Voltage (V_{OUT} = 3.3 V, I_{OUT} = 0 mA)



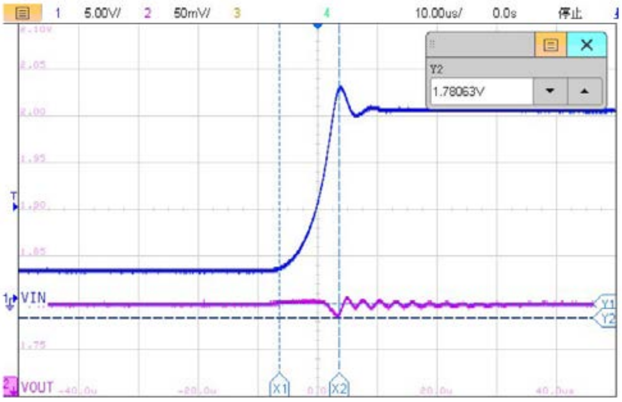
Turn On VS. EN Voltage (V_{OUT} = 5.0 V, I_{OUT} = 0 mA)



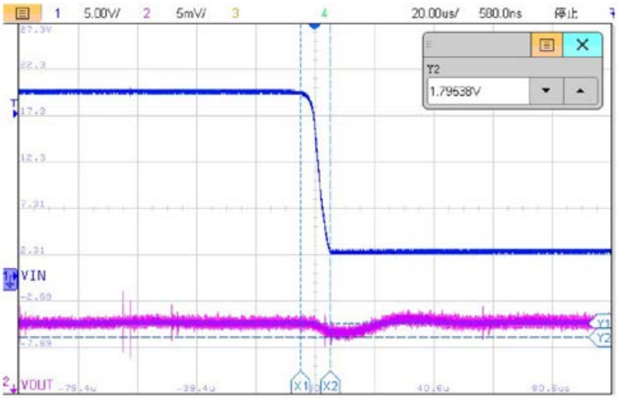
Turn Off VS. EN Voltage (V_{OUT} = 5.0 V, I_{OUT} = 0 mA)

Input Transient Response

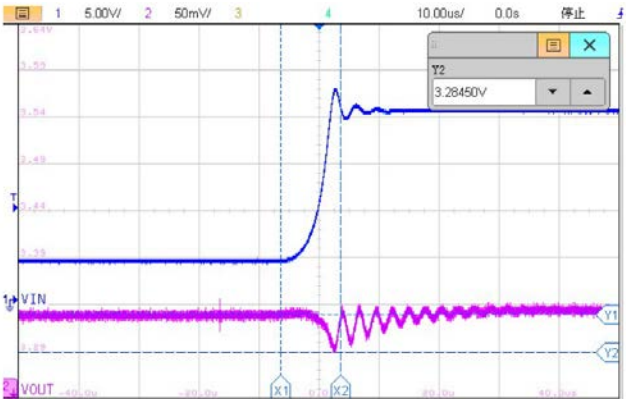
$V_{IN} = V_{OUT} + 1$ V, $C_{OUT} = 10$ μF, t = 10 μs, $I_{OUT} = 10$ mA, V_{IN} jump from 6 V to 18 V



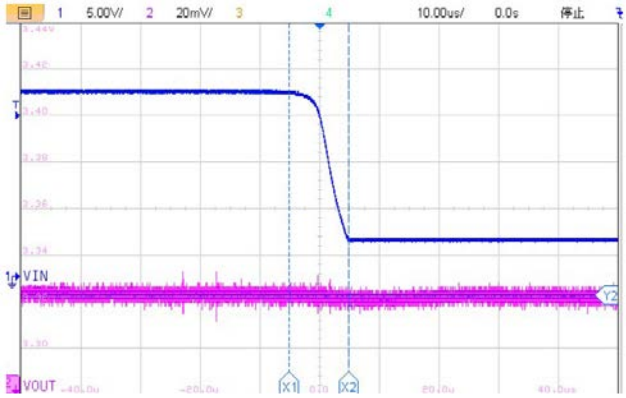
Input Transient Response ($V_{OUT} = 1.8$ V, $I_{OUT} = 1$ mA)



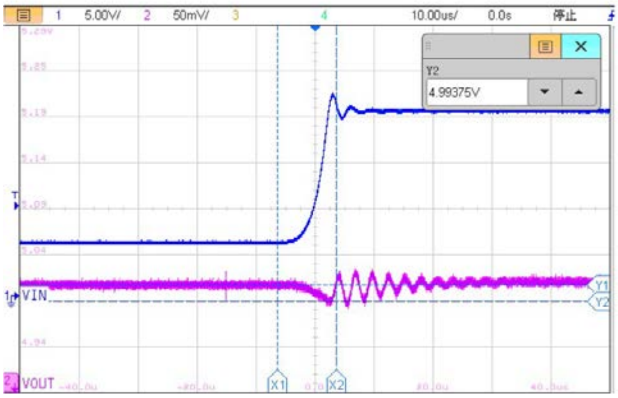
Input Transient Response ($V_{OUT} = 1.8$ V, $I_{OUT} = 1$ mA)



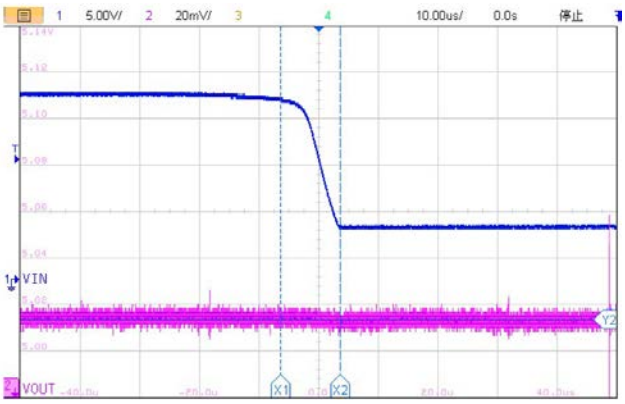
Input Transient Response ($V_{OUT} = 3.3$ V, $I_{OUT} = 1$ mA)



Input Transient Response ($V_{OUT} = 3.3$ V, $I_{OUT} = 1$ mA)



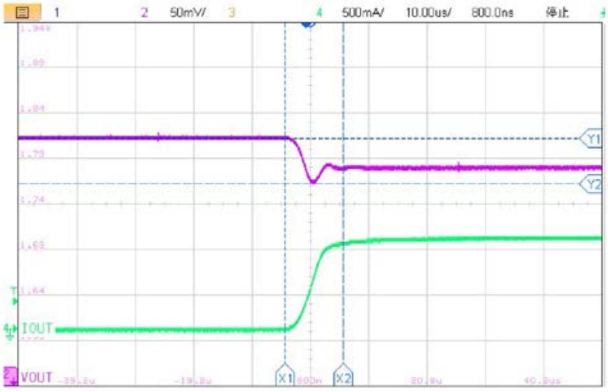
Input Transient Response ($V_{OUT} = 5.0$ V, $I_{OUT} = 1$ mA)



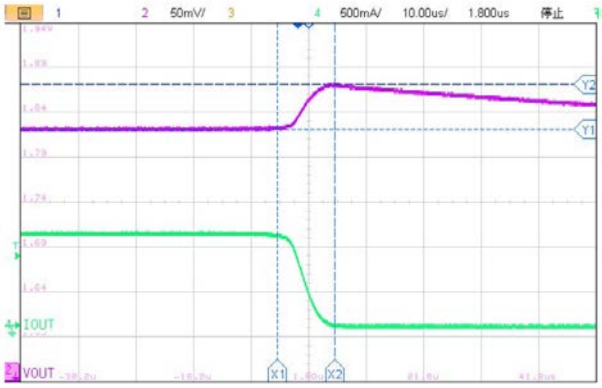
Input Transient Response ($V_{OUT} = 5.0$ V, $I_{OUT} = 1$ mA)

Load Transient Response

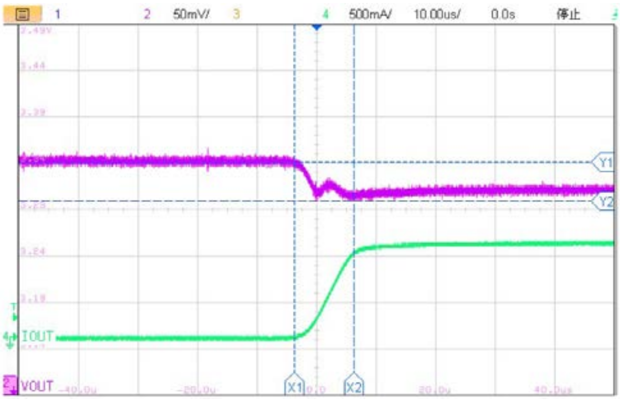
$V_{IN} = V_{OUT} + 1$ V, t = 10 μs, I_{OUT} jump from 1 mA to 1000 mA



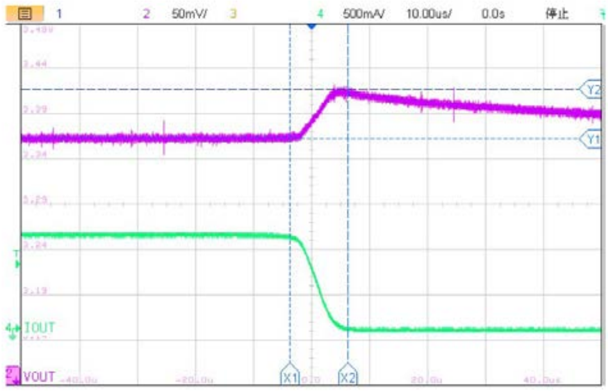
Load Transient Response (V_{OUT} = 1.8 V, I_{OUT} = 1~1000 mA)



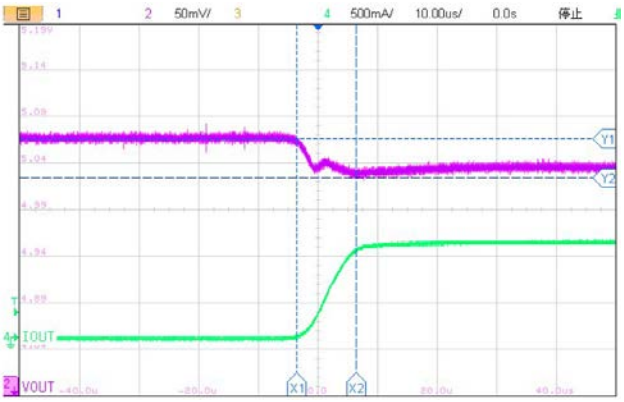
Load Transient Response (V_{OUT} = 1.8 V, I_{OUT} = 1~1000 mA)



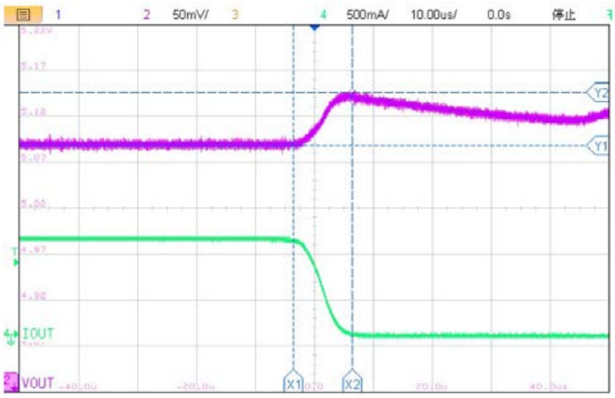
Load Transient Response (V_{OUT} = 3.3 V, I_{OUT} = 1~1000 mA)



Load Transient Response (V_{OUT} = 3.3 V, I_{OUT} = 1~1000 mA)

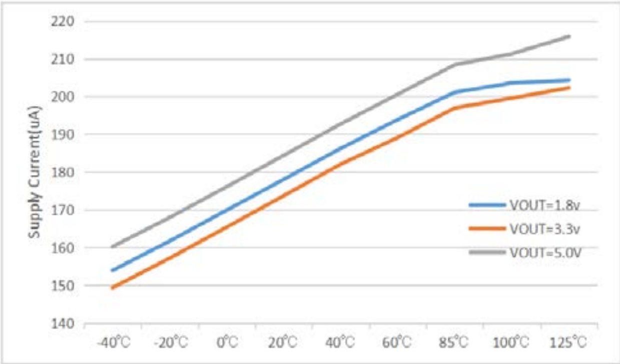


Load Transient Response (V_{OUT} = 5.0 V, I_{OUT} = 1~1000 mA)

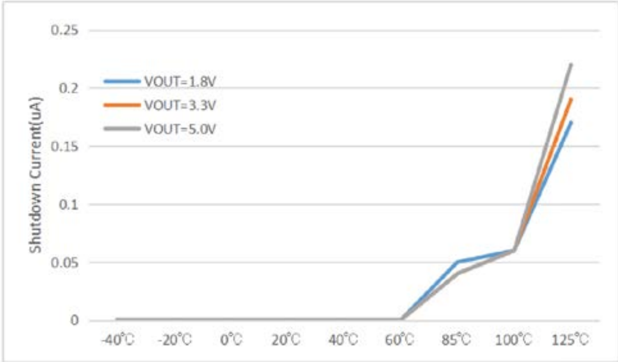


Load Transient Response (V_{OUT} = 5.0 V, I_{OUT} = 1~1000 mA)

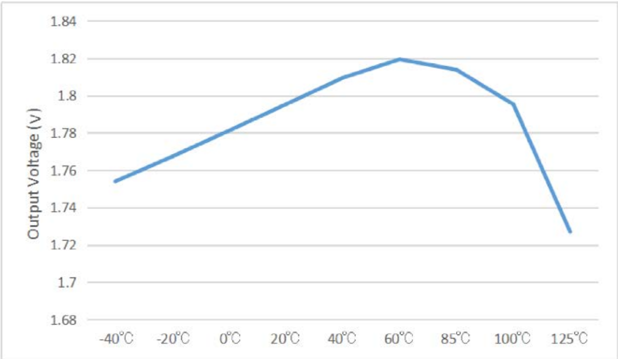
Temperature Characteristics



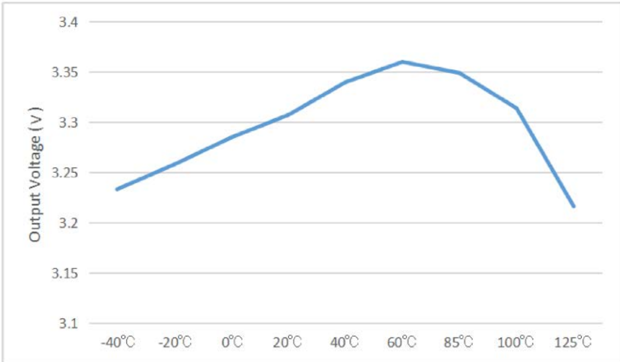
Supply Current VS. Temperature



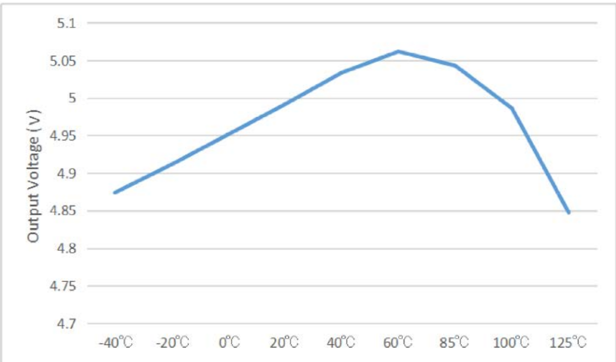
Shutdown Current VS. Temperature



Output Voltage VS. Temperature (V_{OUT} = 1.8 V)



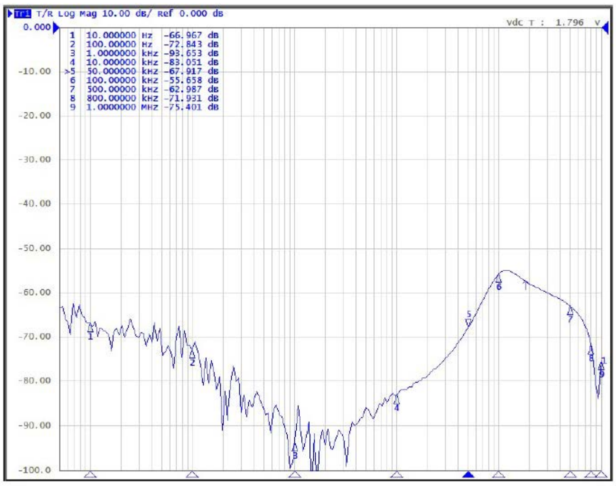
Output Voltage VS. Temperature (V_{OUT} = 3.3 V)



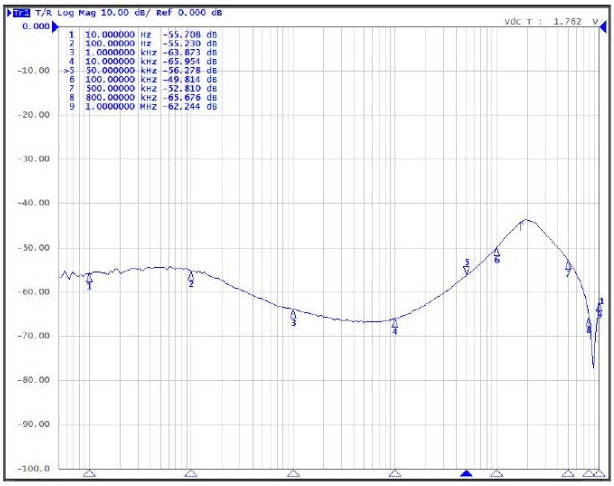
Output Voltage VS. Temperature (V_{OUT} = 5.0 V)

PSRR

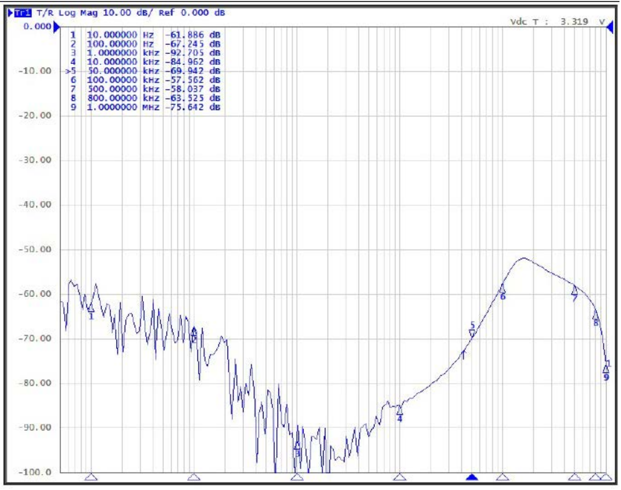
$V_{IN} = V_{OUT} + 1$ V, $I_{OUT} = 0$ mA, $C_{IN} = C_{OUT} = 10$ μF



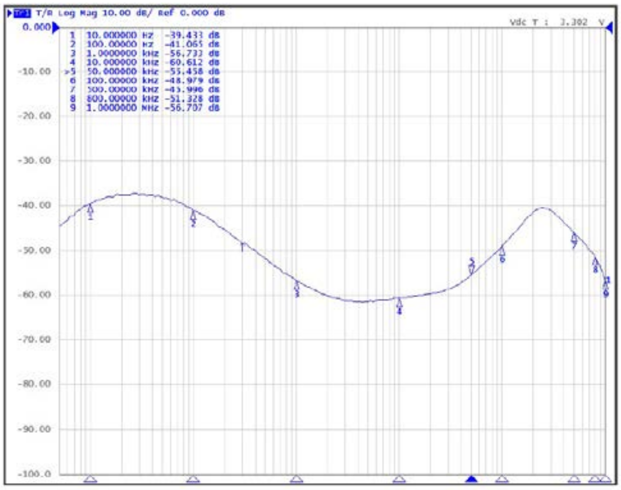
PSRR VS. I_{OUT} ($V_{OUT} = 1.8$ V, $I_{OUT} = 50$ mA)



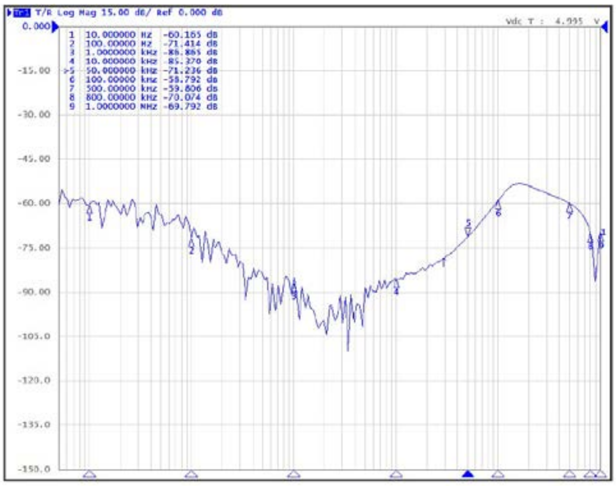
PSRR VS. I_{OUT} ($V_{OUT} = 1.8$ V, $I_{OUT} = 500$ mA)



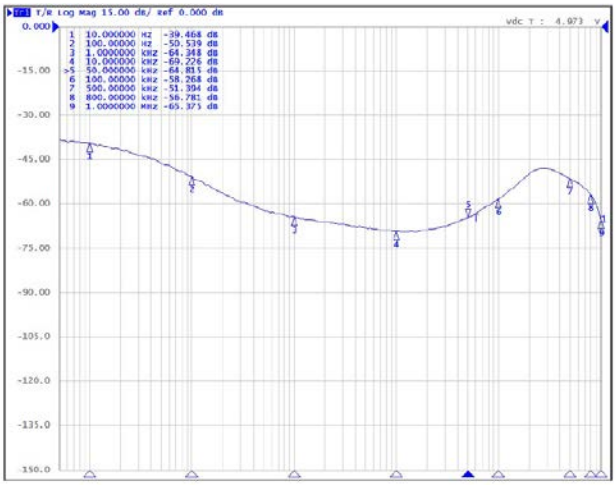
PSRR VS.. I_{OUT} ($V_{OUT} = 3.3$ V, $I_{OUT} = 50$ mA)



PSRR VS. I_{OUT} ($V_{OUT} = 3.3$ V, $I_{OUT} = 500$ mA)

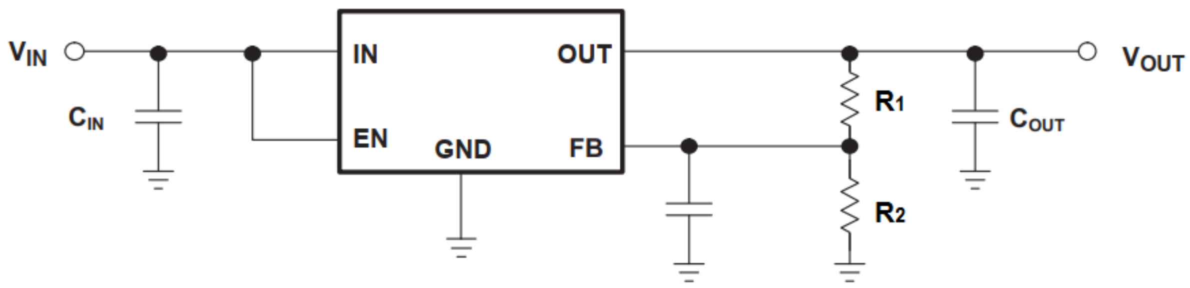


PSRR VS. I_{OUT} ($V_{OUT} = 5.0$ V, $I_{OUT} = 50$ mA)



PSRR VS. I_{OUT} ($V_{OUT} = 5.0$ V, $I_{OUT} = 500$ mA)

APPLICATION CIRCUITS



APPLICATION INFORMATION

Input and Output Capacitor Selection

The SUM3563 requires an output capacitance of 1 μF or larger for stability. Use X5R-type and X7R-type ceramic capacitors because these capacitors have minimal variation in value and equivalent series resistance (ESR) over temperature. When choosing a capacitor for a specific application, pay attention to the dc bias characteristics for the capacitor. Higher output voltages cause a significant derating of the capacitor.

Although an input capacitor is not required for stability, good analog design practice is to connect a capacitor from IN to GND. Some input supplies have a high impedance, thus placing the input capacitor on the input supply helps reduce the input impedance. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. If the input supply has a high impedance over a large range of frequencies, several input capacitors can be used in parallel to lower the impedance over frequency. Use a higher-value capacitor if large, fast, rise-time load transients are anticipated, or if the device is located several inches from the input power source.

Application of Electrolytic Capacitor

If the electrolytic capacitor should be used as input and output capacitor, the capacitance of the capacitor must be greater. The capacity value must be greater than 22 μF.

Enable

The SUM3563 has an EN pin to turn on or turn off the regulator, When the EN pin is in logic high, the regulator will be turned on. The shutdown current is almost 0 μA typical. The EN pin may be directly tied to V_{IN} to keep the part on. The Enable input is CMOS logic and cannot be left floating.

Setting the Output Voltage

The SUM3563 develops a 0.64 V reference voltage, V_{FB}, between the output and the adjust terminal. This voltage is applied across resistor R_1 to generate a constant current. The current I_{ADJ} from the ADJ terminal could introduce DC offset to the output. Because, this offset is very small (about 0.1 μA) , it can be ignored. The constant current then flows through the output set resistor R_2 and sets the output voltage to the desired level. Equation 2 is used for calculating V_{OUT}:

$$V_{OUT} = V_{FB} \times (1 + R_1/R_2) \quad (2)$$

Although I_{ADJ} is very small, $R_1 + R_2$ should be limited to less than 100 kΩ for optimum performance.

Dropout Voltage

The SUM3563 uses a PMOS pass transistor to achieve low dropout. When (V_{IN} - V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} scales approximately with output current because the PMOS device behaves like a resistor in dropout mode. As with any linear regulator, PSRR and transient response degrade as (V_{IN} - V_{OUT}) approaches dropout operation.

Thermal Shutdown

Thermal shutdown protection disables the output when the junction temperature rises to approximately 150℃ Disabling the device eliminates the power dissipated by the device, allowing the device to cool. When the junction temperature cools to approximately 125°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits regulator dissipation, protecting the LDO from damage as a result of overheating. Activating the thermal shutdown feature usually indicates excessive power dissipation as a result of the product of the (V_{IN} - V_{OUT}) voltage and the load current. For reliable operation, limit junction temperature to 125°C maximum.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

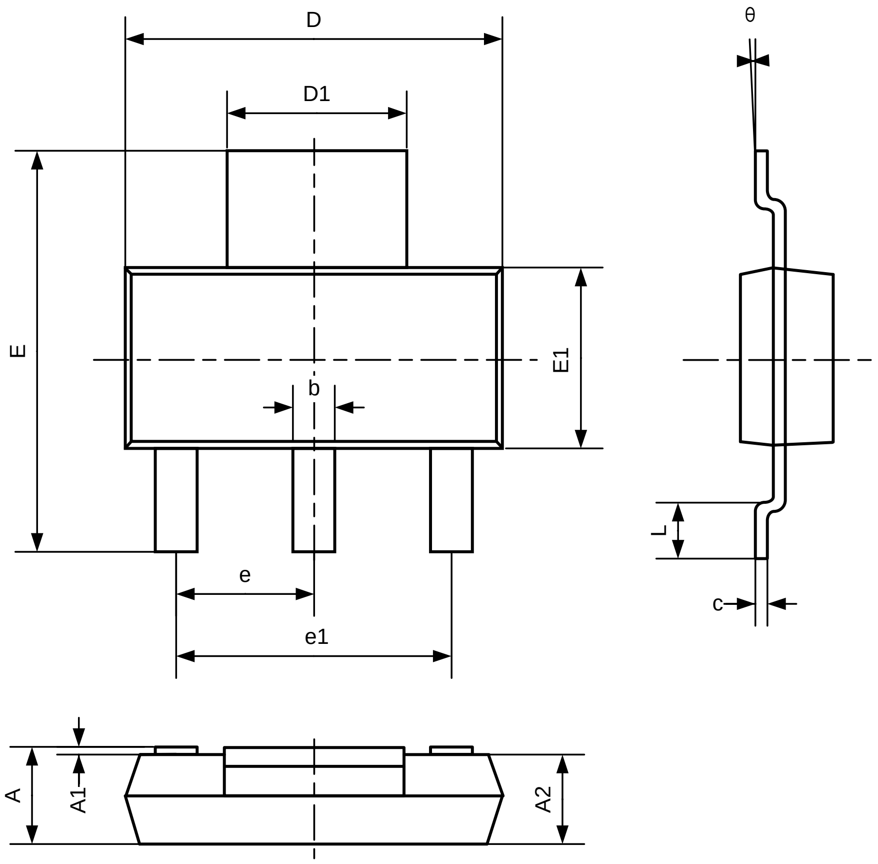
where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications the maximum junction temperature is 125°C and T_A is the ambient temperature. The junction to ambient thermal resistance, θ_{JA}, is layout dependent.

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 6 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

PACKAGE OUTLINE

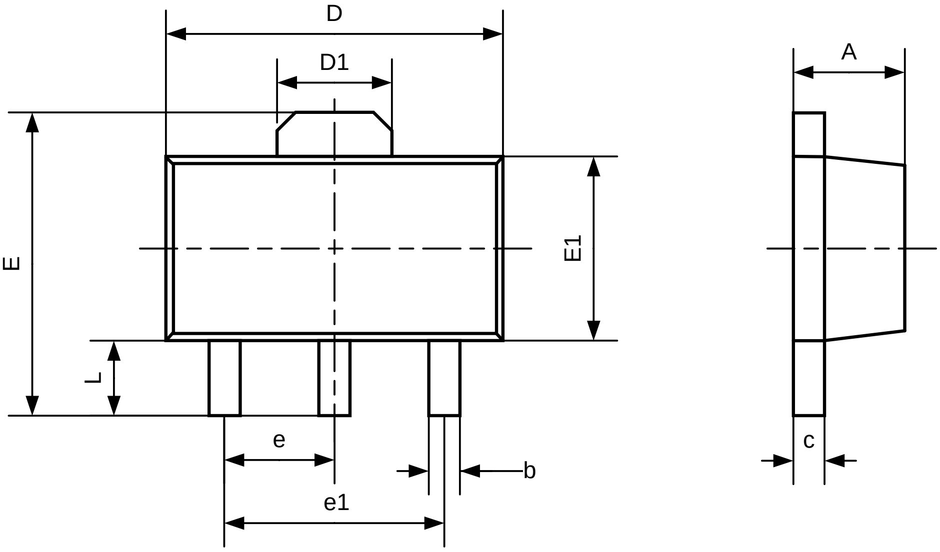
SOT-223



Symbol	Dimensions In Millimeters	
	Min	Max
A	1.520	1.800
A1	0.000	0.100
A2	1.500	1.700
b	0.660	0.820
c	0.250	0.350
D	6.200	6.400
D1	2.900	3.100
E	6.830	7.070
E1	3.300	3.700
e	2.300BSC	
e1	4.500	4.700
L	0.900	1.150
θ	0°	10°

PACKAGE OUTLINE

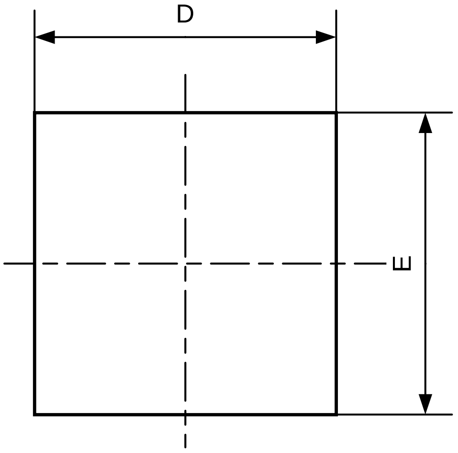
SOT89-3



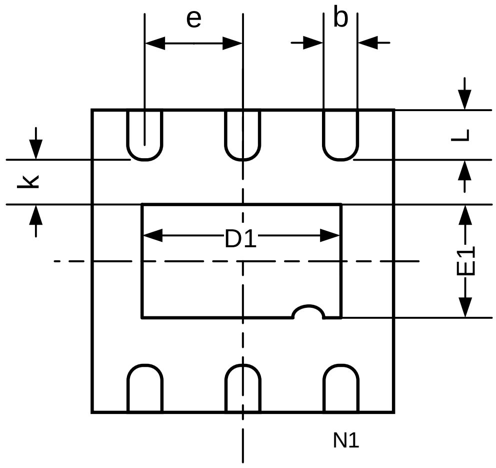
Symbol	Dimensions In Millimeters	
	Min	**Max**
A	1.400	1.600
b	0.320	0.520
c	0.350	0.440
D	4.400	4.600
D1	1.550REF	
E	3.940	4.250
E1	2.300	2.600
e	1.500BSC	
e1	3.000BSC	
L	0.900	1.200

PACKAGE OUTLINE

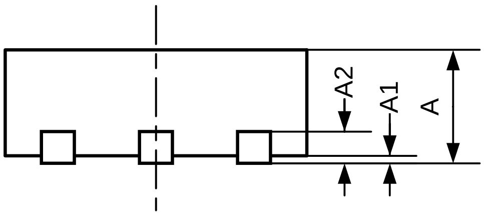
DFN2 × 2-6



TOP VIEW



BOTTOM VIEW

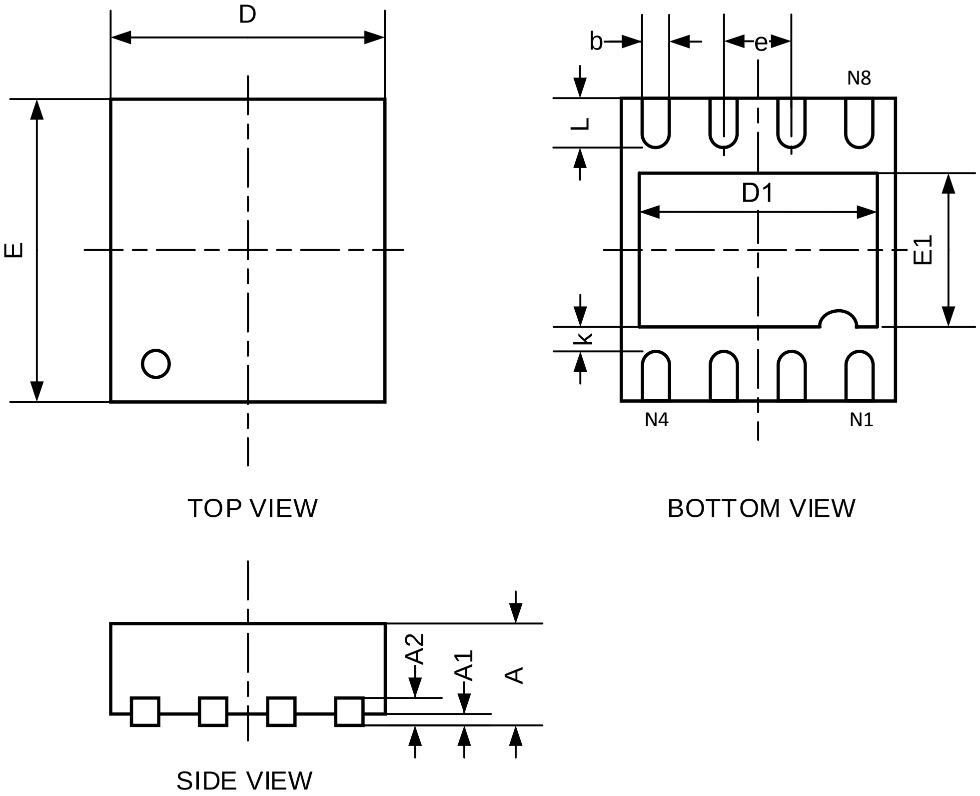


SIDE VIEW

Symbol	Dimensions In Millimeters	
	Min	**Max**
A	0.700	0.900
A1	0.000	0.050
A2	0.203REF	
b	0.180	0.300
D	1.900	2.100
D1	1.100	1.300
E	1.900	2.100
E1	0.600	0.800
e	0.650BSC	
L	0.250	0.450
k	0.200	

PACKAGE OUTLINE

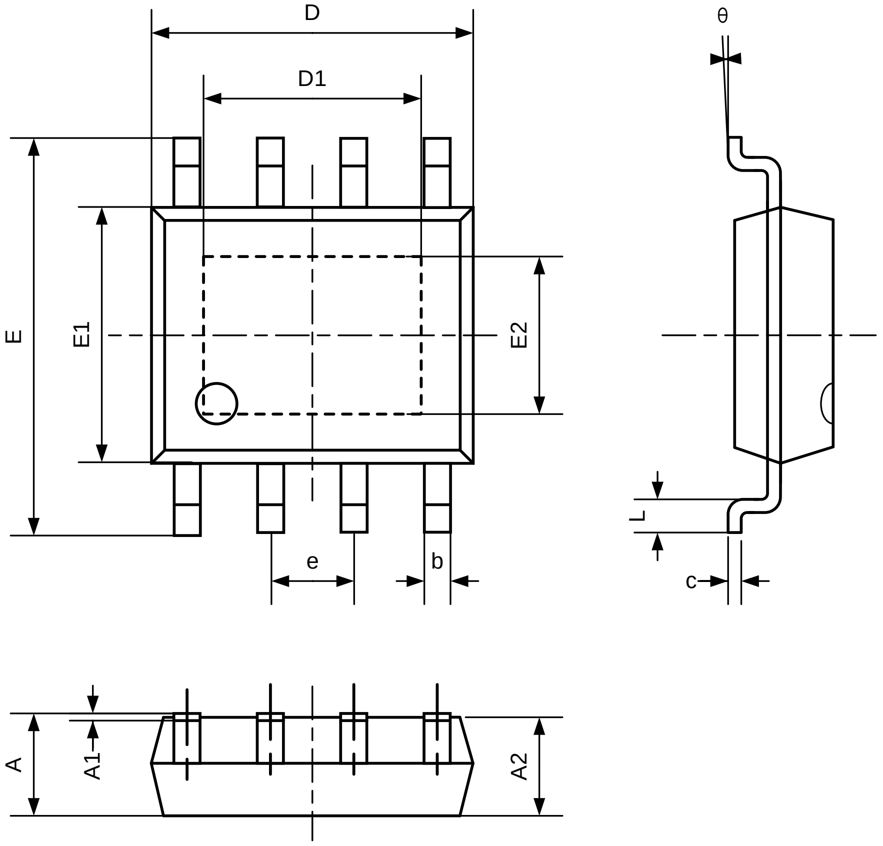
DFN3 × 3-8



Symbol	Dimensions In Millimeters	
	Min	**Max**
A	0.700	0.800
A1	0.000	0.050
A2	0.203REF	
b	0.180	0.300
D	2.900	3.100
D1	2.200	2.400
E	2.900	3.100
E1	1.400	1.600
e	0.650BSC	
L	0.375	0.575
k	0.200	

PACKAGE OUTLINE

ESOP-8



Symbol	Dimensions In Millimeters	
	Min	Max
A		1.750
A1	0.100	0.225
A2	1.300	1.500
b	0.390	0.480
c	0.210	0.260
D	4.700	5.100
D1	3.200	3.400
E	5.800	6.200
E1	3.700	4.100
E2	2.300	2.500
e	1.270BSC	
L	0.500	0.800
θ	0°	8°

V 1.8