High Voltage, Low Power LDO

DESCRIPTION

The SUM3564 is a high voltage, low power consumption and high performance LDO. The family uses an advanced CMOS process and a PMOSFET pass device to achieve fast start-up, with high output voltage accuracy. The SUM3564 is stable with a 1.0 μF ~ 10 μF ceramic output capacitor, and uses a precision voltage reference and feedback loop to achieve a worst-case accuracy of 2% over all load, line, process and temperature variations.

FEATURES

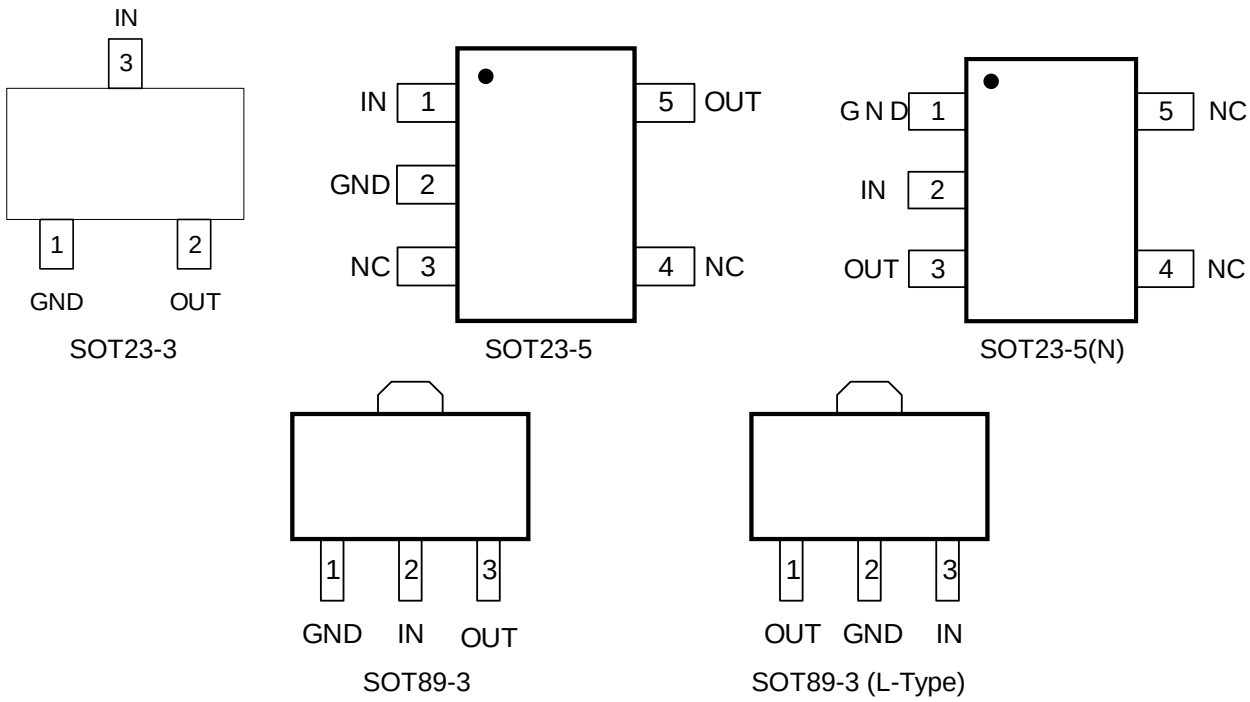
- Wide Input Voltage Range: up to 26 V
- Output Current: 150 mA
- Standard Fixed Output Voltage Options: 2.5 V, 3.0 V, 3.3 V, 4.0 V and 5.0 V
- Other Output Voltage Options Available on Request
- Low I_Q: 1.5 μA
- Low Dropout Voltage
- Short current protection
- Excellent Load/Line Transient Response
- Package: SOT23-3, SOT23-5, SOT23-5(N), SOT89-3, SOT89-3 (L-Type)

ORDER INFORMATION

Model	Package	Ordering Number	Packing Option
SUM3564	SOT23-3	SUM3564-XXKA3	Tape and Reel, 3000
	SOT23-5	SUM3564-XXKA5	Tape and Reel, 3000
	SOT23-5(N)	SUM3564-XXKA5N	Tape and Reel, 3000
	SOT89-3	SUM3564-XXP	Tape and Reel, 1000
	SOT89-3 (L-Type)	SUM3564-XXPL	Tape and Reel, 1000

*XX: When expressed as 33, the output voltage is 3.3 V; when expressed as 50 the output voltage is 5.0 V.

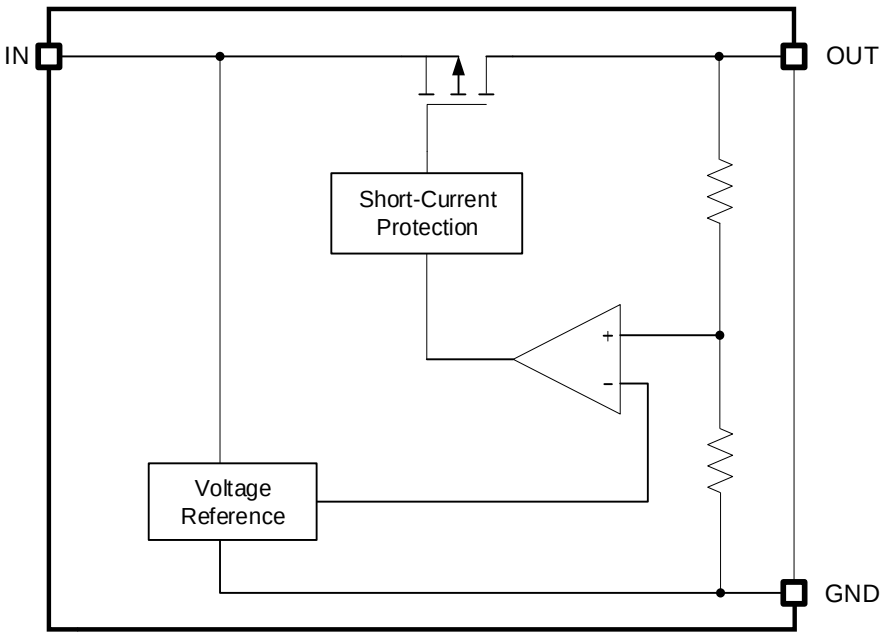
PIN CONFIGURATION (Top View)



PIN DESCRIPTIONS

Pin					Symbol	Description
SOT23-3	SOT23-5	SOT23-5(N)	SOT89-3	SOT89-3 (L-Type)		
2	5	3	3	1	OUT	Output pin.
1	2	1	1	2	GND	Ground.
3	1	2	2	3	IN	Supply input pin.
	3, 4	4, 5			NC	No connection.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Input Capacitor

A 1 μF ~ 10 μF ceramic capacitor is recommended to connect between V_{IN} and GND pins to decouple input power supply glitch and noise. The amount of the capacitance may be increased without limit. This input capacitor must be located as close as possible to the device to assure input stability and less noise. For PCB layout, a wide copper trace is required for both V_{IN} and GND.

Output Capacitor

An output capacitor is required for the stability of the LDO. The recommended output capacitance is from 1 μF to 10 μF, Equivalent Series Resistance (ESR) is from 5 mΩ to 100 mΩ, and temperature characteristics are X7R or X5R. Higher capacitance values help to improve load/line transient response. The output capacitance may be increased to keep low undershoot/overshoot. Place output capacitor as close as possible to OUT and GND pins.

Low Quiescent Current

The SUM3564, consuming only around 1.5 μA for all input range and output loading, provides great power saving in portable and low power applications.

Short Current Limit Protection

When output current at the OUT pin is higher than current limit threshold or the OUT pin is short-circuit to GND, the short current limit protection will be triggered and clamp the output current to approximately 20 mA to prevent over-current and to protect the regulator from damage due to overheating.

ABSOLUTE MAXIMUM RATINGS(2)

Parameter	Rating		Unit
IN pin to GND pin	-0.3 to 30		V
Thermal Resistance (Junction to Ambient) (1)	SOT23-3	360	°C/W
	SOT23-5	250	
	SOT89-3	135	
Junction Temperature	150		°C
Storage Temperature	-65 to 150		°C
Lead Temperature (Soldering, 10 sec)	300		°C
ESD (HBM mode), ESDA/JEDEC JS-001-2017	±2000		V

NOTE:

(1) This particular frame decreases the total thermal resistance of the package and increases its ability to dissipate power when an appropriate area of copper on the printed circuit board is available for heat-sinking.

(2) Stresses beyond those listed under “ABSOLUTE MAXIMUM RATINGS” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Rating	Unit
Operation Temperature range	-40 to 85	°C

CAUTION

This integrated circuit can be damaged by ESD if you don’t pay attention to ESD protection. SUMSEMI recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications. SUMSEMI reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time. Please contact SUMSEMI sales office to get the latest datasheet.

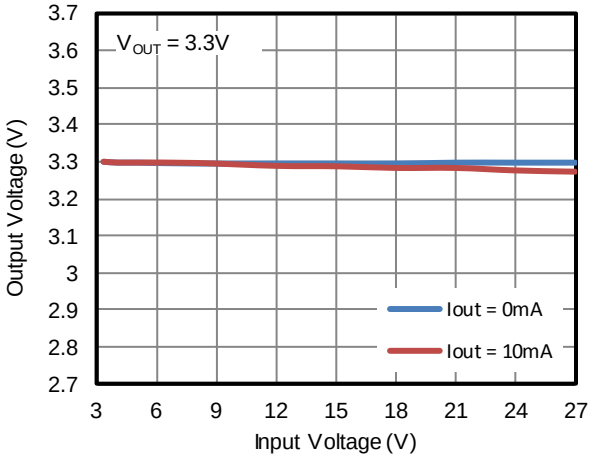
ELECTRICAL CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

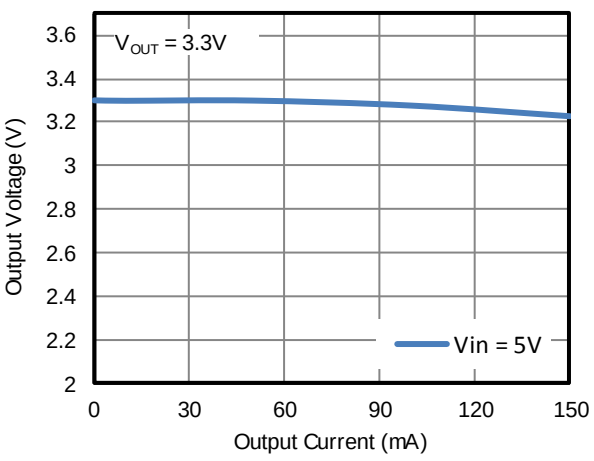
Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Input Voltage Operation Range	V_{IN}					26	V
Dropout Voltage	V_{DROP}	I_{OUT} = 50 mA, V_{OUT} = 3.3 V Δ V_{OUT} = ±2%*V_{OUT}		300	360	420	mV
		I_{OUT} = 100 mA, V_{OUT} = 3.3 V Δ V_{OUT} = ±2%*V_{OUT}		600	700	800	
DC Supply Quiescent Current	I_Q	I_{OUT} = 0 mA, V_{IN} < 28 V			1.5	5	μA
Regulated Output Voltage	V_{OUT}	I_{OUT} = 1 mA		V_{OUT} × 0.98		V_{OUT} × 1.02	V
Output Voltage Line Regulation	Δ V_{OUT}	V_{IN} = V_{OUT} + 1 V to 24 V, I_{OUT} = 10 mA		-15		15	mV
Output Voltage Load Regulation	Δ V_{OUT}	V_{IN} = V_{OUT} + 1.5 V , I_{OUT} from 1 mA to 100 mA V_{IN} ≤ 26 V		-50		50	mV
Maximum Output Current	I_{OUT}	V_{IN} = V_{OUT} + 1.5 V			150		mA
Power Supply Rejection Ratio	PSRR	I_{OUT} = 10 mA	f = 100 Hz		75		dB
			f = 1 kHz		55		
Short Current	I_{SHORT}	V_{OUT} = 0 V			20		mA

TYPICAL PERFORMANCE CHARACTERISTIC

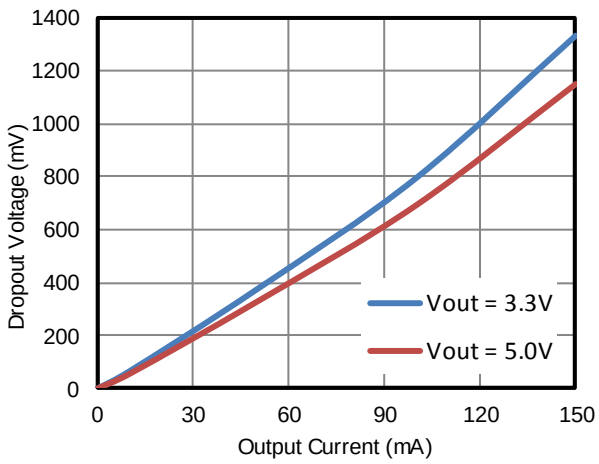
Output Voltage vs. Input Voltage



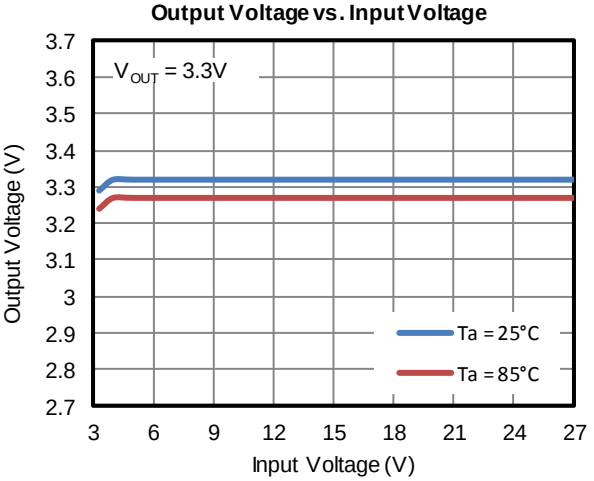
Output Voltage vs. Output Current



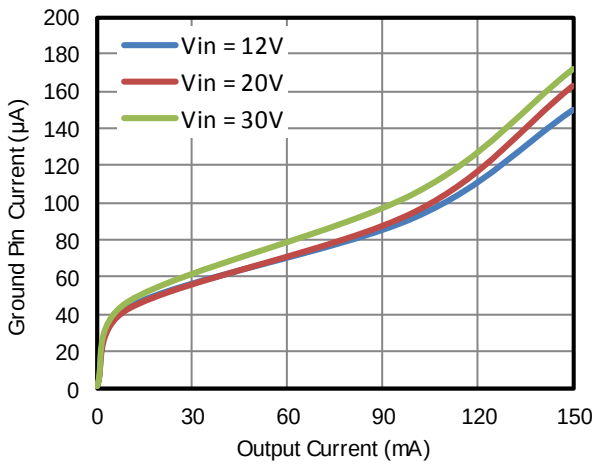
Dropout Voltage vs. Output Current



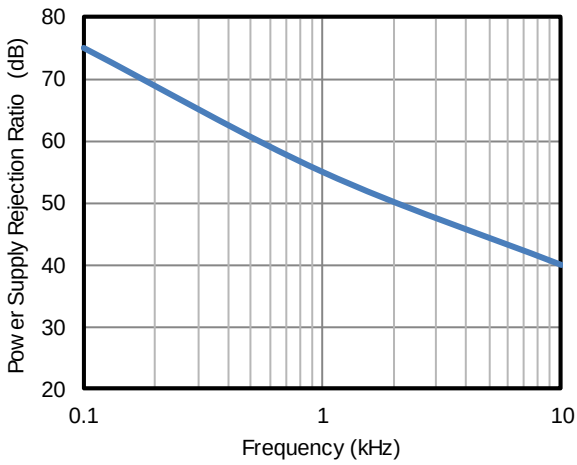
Output Voltage vs. Input Voltage



Ground Pin Current vs. Output Current

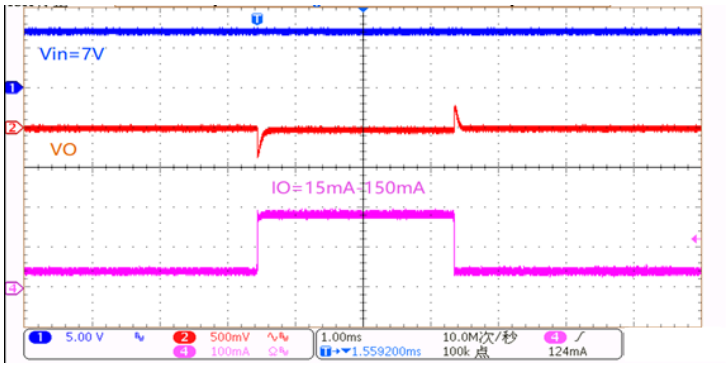


Power Supply Rejection Ratio vs. Frequency



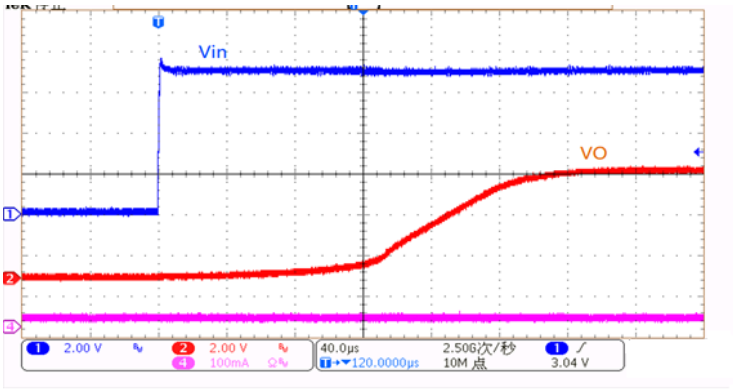
TYPICAL PERFORMANCE CHARACTERISTIC

Load-Transient Response



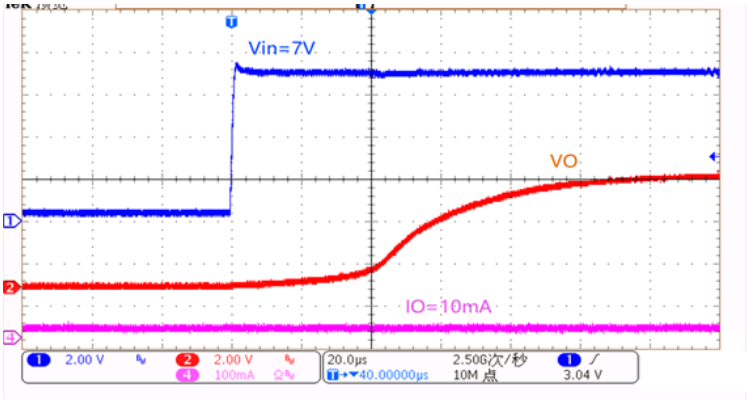
V_{IN} = 7V, C_{IN} = 1μF, C_{OUT} = 1μF

Start up



V_{IN} = 7V, C_{IN} = 1μF, C_{OUT} = 1μF , Load = NA

Start up



V_{IN} = 7V, C_{IN} = 1μF, C_{OUT} = 1μF, Load =10mA

APPLICATION

This series of chips are three terminal low dropout linear regulators. The following application points must be strictly followed for correct operation.

External Circuit

Input and output pins must be connected to external capacitors. For the input pin, especially when high impedance is generated by battery power supply, a suitable bypass capacitor must be connected, it is recommended that the input capacitance value be at least 1 μF, it is also a ceramic capacitor to achieve better temperature coefficient and lower ESR (equivalent series resistance). As shown in the application circuit, for the output pin, especially when the load has transient performance, the appropriate capacitor must be connected, the output capacitor plays an important role in maintaining the stability of the output voltage. For ceramic capacitors, the capacitance value shall be at least 1 μF. Selecting a larger capacitance can limit the transient voltage output.

Thermal Considerations

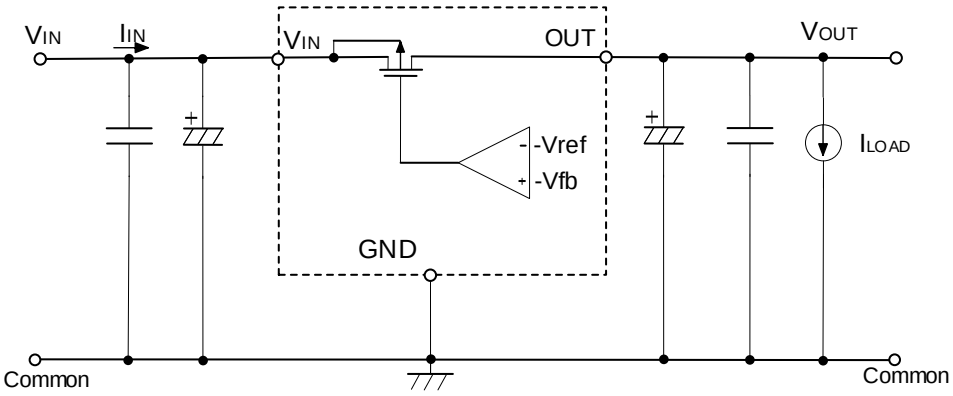
The maximum power consumption of the chip depends on the thermal resistance of the IC package、PCB layout、ambient air velocity and the temperature difference between the node and the ambient temperature. The maximum power consumption can be calculated by the following formula: $PD_{(max)} = (T_{J(max)} - T_A)/ \theta_{JA}$ where $T_{J(max)}$ is the maximum node temperature, T_A is the ambient temperature, and θ_{JA} is the node to ambient thermal resistance per watt degree in IC package. The following table shows the value of various package types θ_{JA}.

PACKAGE	θ_{JA} (℃/W)
SOT23-3	360 ℃/W
SOT23-5	250 ℃/W
SOT89-3	135 ℃/W

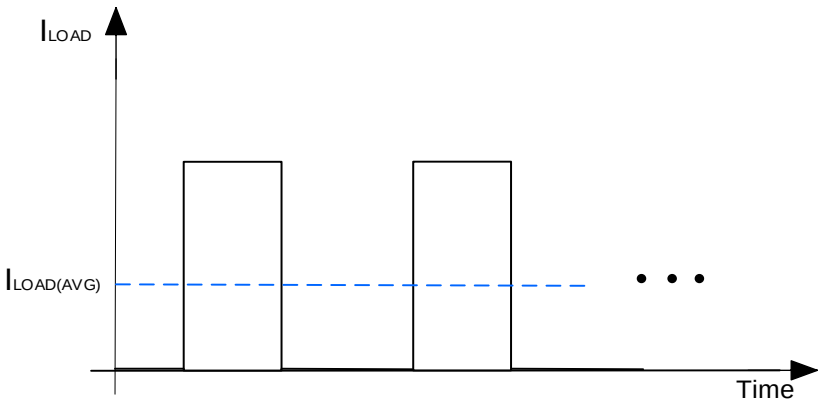
In the working limit parameters, the maximum junction temperature is 150℃. Nevertheless, it is recommended that the maximum junction temperature during normal operation should not exceed 125℃ to ensure its reliability.

Power Consumption Calculation

In order to make the chip work within the limit range and maintain a stable output voltage, the power consumption PD of the chip must not exceed the maximum. High power consumption $PD_{(max)}$, i.e. $PD \leq PD_{(max)}$. As can be seen from the belowing figure, almost all power is generated through transistors, which is equivalent to connecting a variable resistor in series with the load to keep the output voltage constant. The power generated here is expressed as heat energy. It must be ensured that the chip cannot exceed the maximum node temperature.



Due to the transient performance of load, the regulator is required to provide steady-state and transient current in practical application. Although this series of chips operate within the limit range and work well under its steady-state current, we must pay attention to the transient load that may cause the current to rise close to the limit parameters, which will also lead to the increase of chip node temperature. The mean value of the current in the chip and the current generated in the transient state should be considered, more precisely, the RMS value of the current in the chip. The following figure shows the average current associated with the transient current.



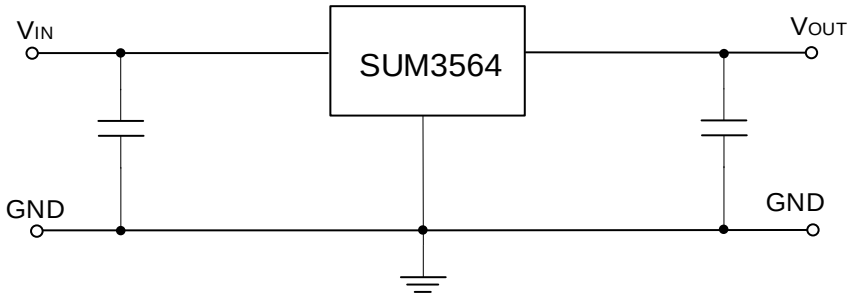
Because the transient current of the chip is very small and can generally be ignored, assuming that the input current is equal to the output current, the power consumption PD of the chip can be calculated as the voltage difference between the input voltage and the output voltage multiplied by the current, and the formula PD = (V_{IN} − V_{OUT}) × I_{IN}, Because the input current is also equal to the load current, the formula PD = (V_{IN} − V_{OUT}) × I_{LOAD}, but due to the existence of transient load current, the power consumption PD should be PD = (V_{IN} − V_{OUT}) × $I_{LOAD(AVG)}$.

Current Protection Function

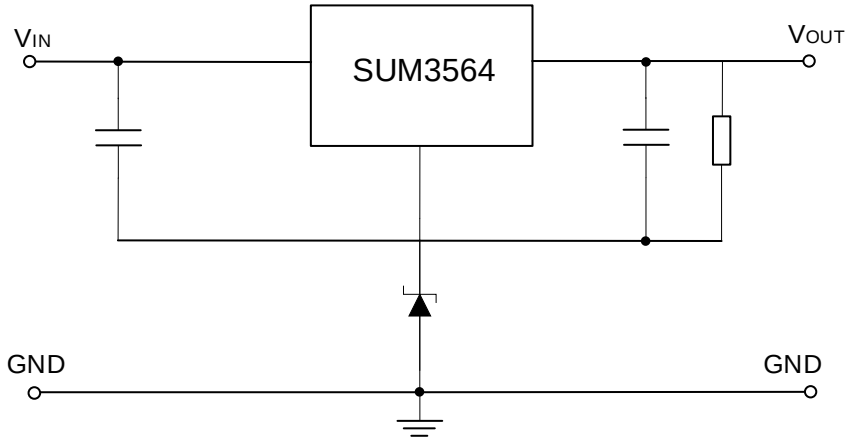
SUM3564 realizes the functions of over-current protection and short-circuit protection. It has 2-level over-current protection threshold. Once the output voltage is greater than 0.7 V, the overcurrent protection function will take effect and the OCP limit current will be set to 180 mA. If the output voltage is lower than 0.7 V, the short-circuit protection function takes effect, and the SCP current is set to 20 mA. Even if the output is short circuited to ground, IC damage can be prevented. When the output is short circuited to ground, the output current will be clamped to I_{SCP}.

APPLICATION CIRCUITS

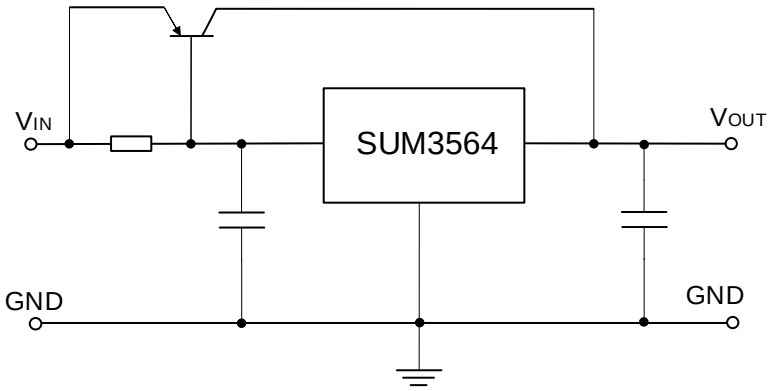
Basic Application Circuit



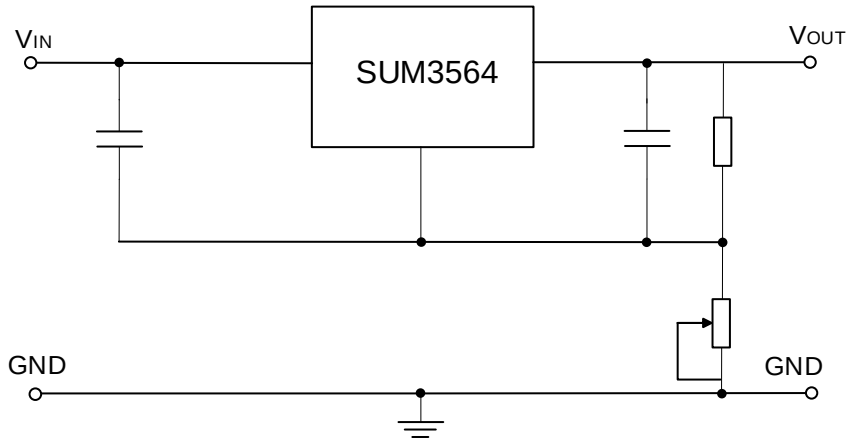
Extended Output Voltage Application Circuit



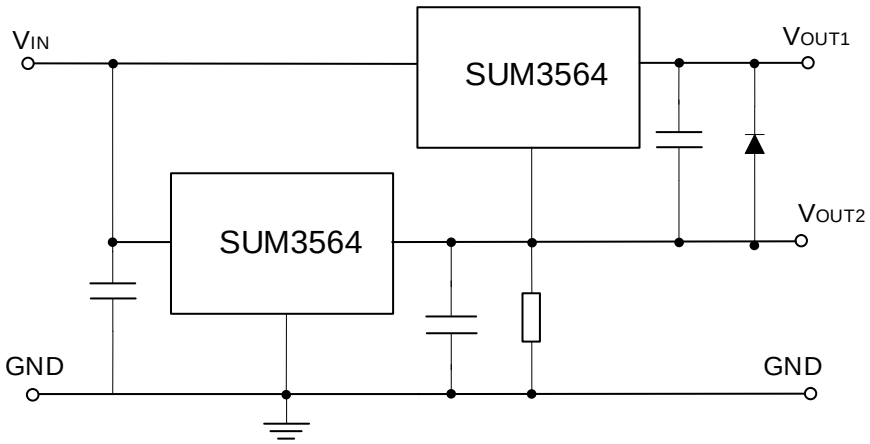
High Output Current Positive Voltage Stabilizing Application Circuit



Constant Current Source Output Application Circuit

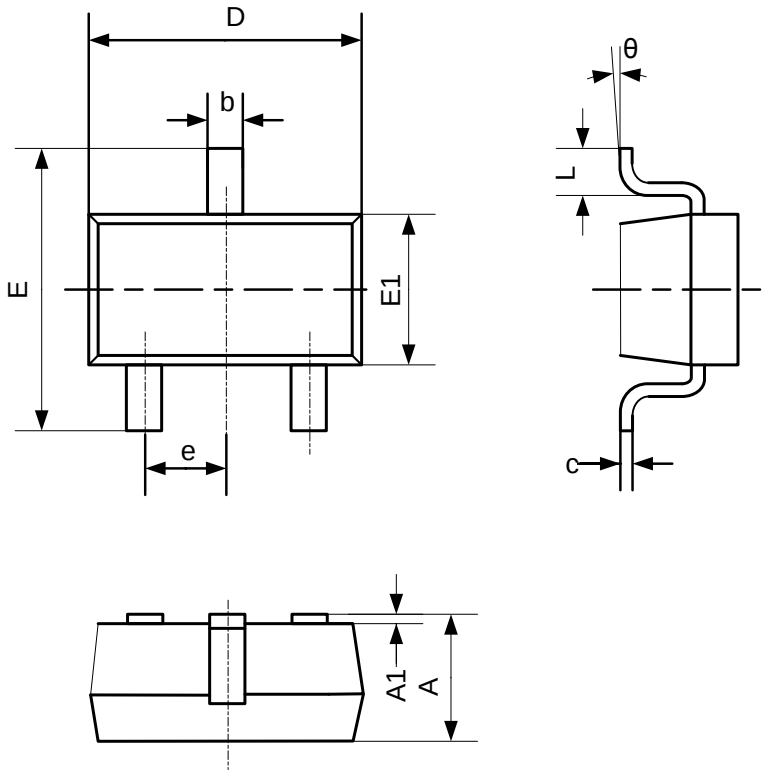


Dual Channel Output Application Circuit



PACKAGE OUTLINE

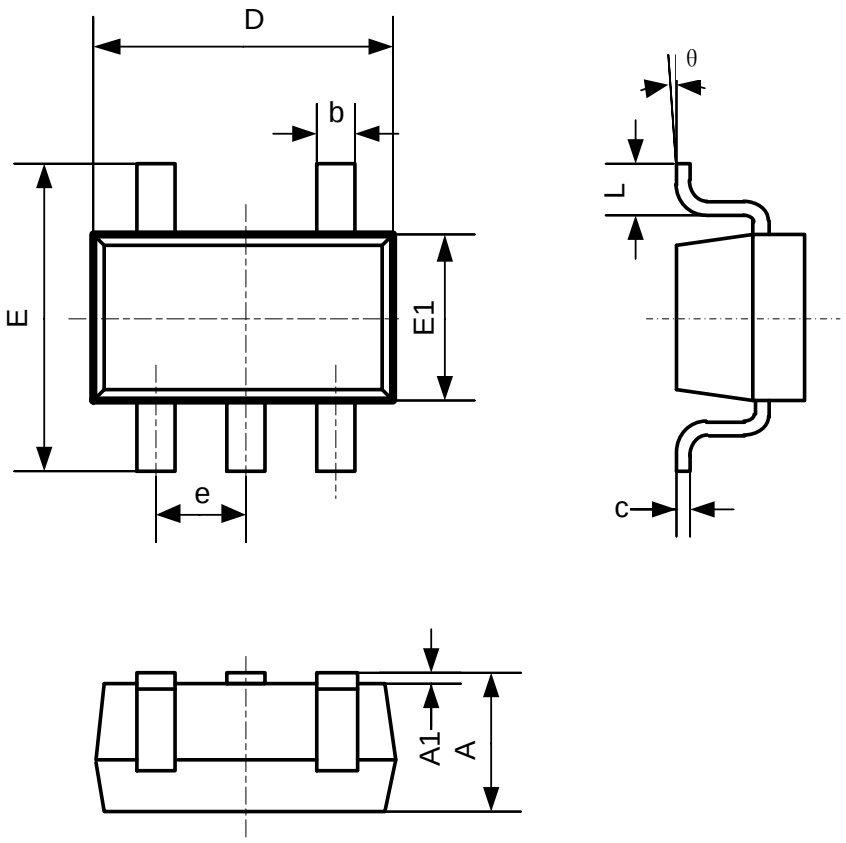
SOT23-3



Symbol	Dimensions In Millimeters	
	Min	Max
A	1.050	1.250
A1	0.000	0.100
b	0.300	0.500
c	0.100	0.200
D	2.820	3.020
E	2.650	2.950
E1	1.500	1.700
e	0.950BSC	
L	0.300	0.600
θ	0°	8°

PACKAGE OUTLINE

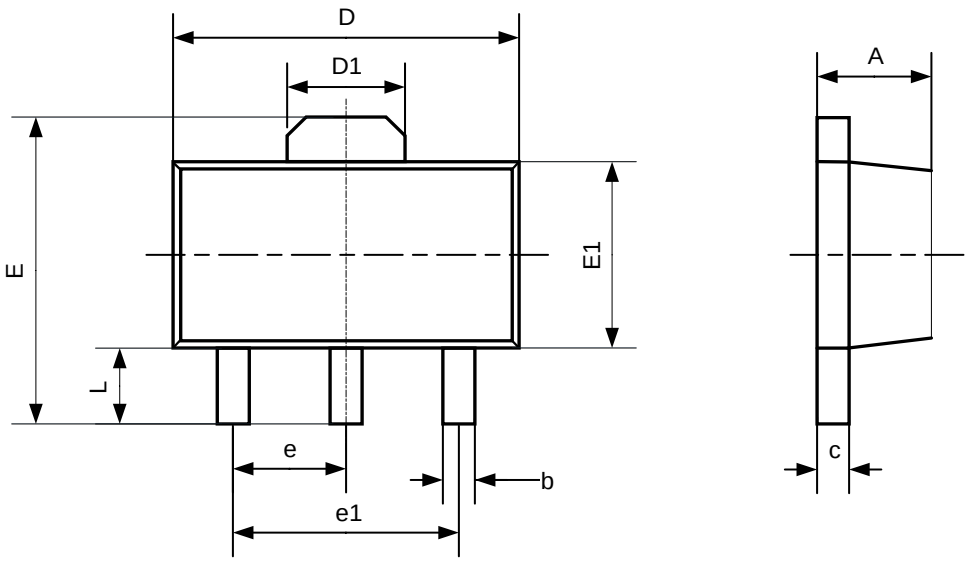
SOT23-5



Symbol	Dimensions In Millimeters	
	Min	Max
A	1.05	1.25
A1	0.00	0.10
b	0.35	0.50
c	0.08	0.20
D	2.82	3.02
E	2.60	3.00
E1	1.60	1.70
e	0.95BSC	
L	0.30	0.60
θ	0°	8°

PACKAGE OUTLINE

SOT89-3



Symbol	Dimensions In Millimeters	
	Min	Max
A	1.400	1.600
b	0.320	0.520
c	0.350	0.440
D	4.400	4.600
D1	1.550REF	
E	3.940	4.250
E1	2.300	2.600
e	1.500BSC	
e1	3.000BSC	
L	0.900	1.200