High Input Ultra-high PSRR 300mA LDO

DESCRIPTION

SUM3565 is a high input voltage and ultra high PSRR 300 mA LDO with enable function that output adjustable from 1.0 V ~ 5 V, is designed specifically for portable battery-powered applications which require low quiescent current. The consumption of type 50 uA ensures long battery life and dynamic transient boost feature improves device transient response for wireless communication applications.

SUM3565 is offered SOT23-5 package.

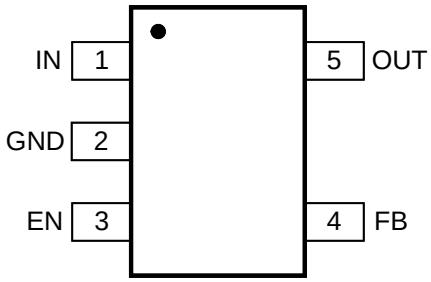
FEATURES

- Wide input voltage range from 3 V to 24 V
- Up to 300 mA Load Current
- I_Q is 50 µA typical
- ADJ Output Voltage range 1.0 V ~ 5.0 V
- Very Low dropout is 330 mV at 150 mA Load @ V_{OUT} = 3.3V
- Excellent load/line transient response
- Ultra High Ripple Rejection: 90 dB at 1 KHz
- Package is SOT23-5

ORDER INFORMATION

Model	Package	Ordering Number	Packing Option
SUM3565-ADJ	SOT23-5	SUM3565-ADJKA5	Tape and Reel, 3000

PIN CONFIGURATION (Top View)

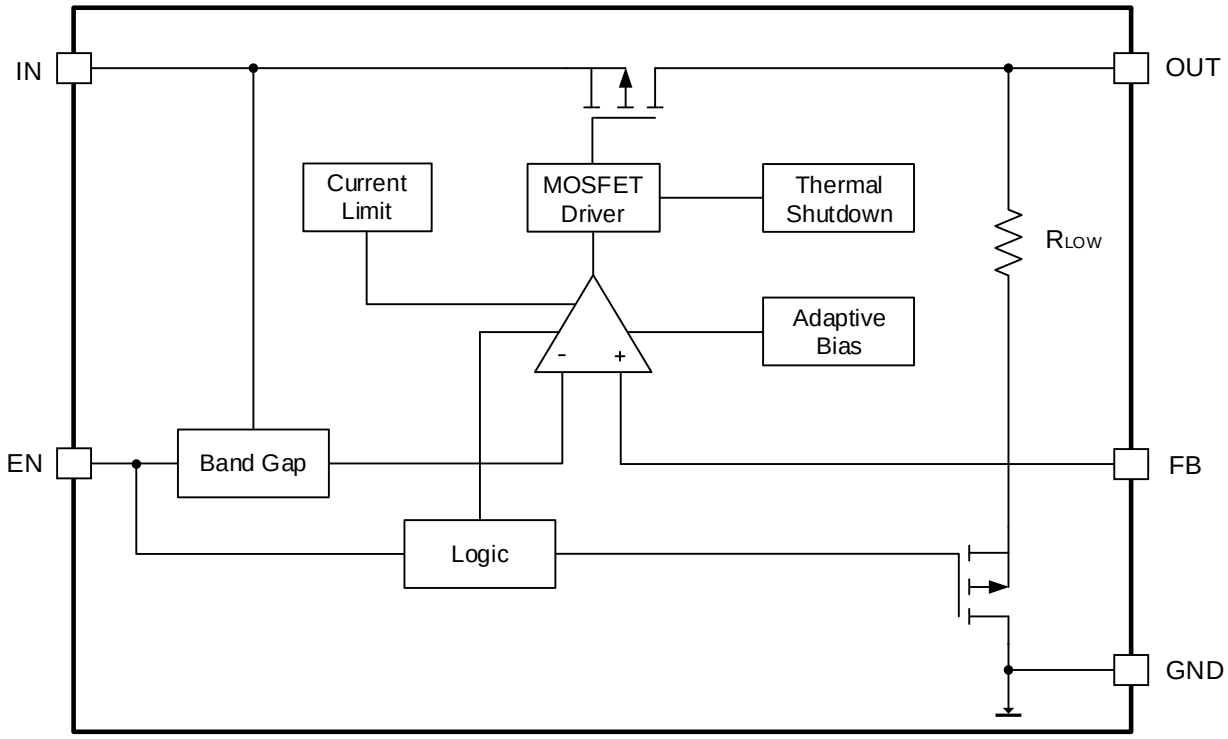


SOT23-5

PIN DESCRIPTIONS

Pin	Symbol	Description
1	IN	Supply input pin.
2	GND	Ground.
3	EN	Enable control input, active high.
4	FB	Set the output voltage.
5	OUT	Output pin.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

INPUT CAPACITOR

A 1 μF ~ 10 μF ceramic capacitor is recommended to connect between IN and GND pins to decouple input power supply glitch and noise. The amount of the capacitance may be increased without limit. This input capacitor must be located as close as possible to the device to assure input stability and less noise. For PCB layout, a wide copper trace is required for both IN and GND.

OUTPUT CAPACITOR

An output capacitor is required for the stability of the LDO. The recommended output capacitance is from 1 μF to 10 μF, Equivalent Series Resistance (ESR) is from 5 mΩ to 100 mΩ, and temperature characteristics are X7R or X5R. Higher capacitance values help to improve load/line transient response. The output capacitance may be increased to keep low undershoot/overshoot. Place output capacitor as close as possible to OUT and GND pins.

ENABLE

The SUM3565 delivers the output power when it is set to enable state. When it works in disable state, there is no output power and the operation quiescent current is almost zero. The enable pin (EN) is active high.

DROPUT VOLTAGE

The SUM3565 uses a PMOS pass transistor to achieve low dropout. When (V_{IN} - V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} scales approximately with output current because the PMOS device behaves like a resistor in dropout mode. As with any linear regulator, PSRR and transient response degrade as (V_{IN} - V_{OUT}) approaches dropout operation.

THERMAL SHUTDOWN

Thermal shutdown protection disables the output when the junction temperature rises to approximately 155°C. Disabling the device eliminates the power dissipated by the device, allowing the device to cool. When the junction temperature cools to approximately 130°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits regulator dissipation, protecting the LDO from damage as a result of overheating. Activating the thermal shutdown feature usually indicates excessive power dissipation as a result of the product of the (V_{IN} - V_{OUT}) voltage and the load current. For reliable operation, limit junction temperature to 125°C maximum.

THERMAL CONSIDERATIONS

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

Where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications the maximum junction temperature is 125°C and T_A is the ambient temperature. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For SOT23-5 package, the thermal resistance, θ_{JA}, is 250°C/W on the test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula:

$$P_{D(MAX)} = (125°C - 25°C) / (250°C/W) = 0.4 \text{ W for SOT23-5 package}$$

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}.

CURRENT-LIMIT PROTECTION

The SUM3565 provides current limit function to prevent the device from damages during over-load or shorted-circuit condition. This current is detected by an internal sensing transistor.

Layout Guidelines

- Place input and output capacitors as close to the device as possible.
- Use copper planes for device connections in order to optimize thermal performance.
- Place thermal vias around the device to distribute heat.
- Do not place a thermal via directly beneath the thermal pad of the DRV package. A via can wick solder or solder paste away from the thermal pad joint during the soldering process, leading to a compromised solder joint on the thermal pad.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{IN}	Input Voltage(1)		-0.3 to 30	V
V_{OUT}	Output Voltage		-0.3 to 6	V
V_{EN}	Chip Enable Input		-0.3 to 30	V
$T_{J(MAX)}$	Maximum Junction Temperature		150	°C
T_{STG}	Storage Temperature		-65 to 150	°C
ESD (HBM)	Human Body Model(2)		2000	V
ESD (CDM)	ESD Capability(2)		1500	V
Latch up	Current Maximum Rating(2)		200	mA
$R_{\theta JA}$	Thermal Characteristics, Thermal Resistance, Junction-to-Air	SOT23-5	250	°C/W

NOTES:

Stresses beyond those listed under “ABSOLUTE MAXIMUM RATINGS” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1. Refer to Electrical Characteristics and Application Information for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per EIA/JESD22-A114 ;
   CDM tested per JESD22-C101;
   Latch up Current Maximum Rating tested per JEDEC78.

CAUTION

This integrated circuit can be damaged by ESD if you don’t pay attention to ESD protection. SUMSEMI recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications. SUMSEMI reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time. Please contact SUMSEMI sales office to get the latest datasheet.

RECOMMENDED OPERATING CONDITIONS

Symbol	Item	Rating	Unit
V_{IN}	Input Voltage	3 to 24	V
I_{OUT}	Output Current	0 to 300	mA
T_A	Operating Ambient Temperature	- 40 to 85	°C
C_{IN}	Effective Input Ceramic Capacitor Value	1 to 10	μF
C_{OUT}	Effective Output Ceramic Capacitor Value	1 to 10	μF
ESR	Input and Output Capacitor Equivalent Series Resistance	5 to 100	mΩ

ELECTRICAL CHARACTERISTICS

(V_{IN} = V_{OUT} +2V; I_{OUT} = 10mA, C_{IN} = C_{OUT} = 2.2μF, unless otherwise noted. Typical values are at T_A = +25°C.) (3)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IN}	Operating Input Voltage		3		24	V
V_{FB}	FB Voltage	T_A = +25°C	0.591	0.600	0.609	V
		-40°C ≤ T_A ≤ 85°C	0.588		0.612	
$Line_{REG}$	Line Regulation	V_{OUT} +2 ≤ V_{IN} ≤ 24 V, I_{OUT} = 10 mA		0.05	0.20	%/V
V_{DROP}	DropoutVoltage	I_{OUT} = 300 mA, V_{OUT} = 3.3 V		600	950	mV
	Dropout Voltage	I_{OUT} = 150 mA, V_{OUT} = 3.3 V		270	450	mV
$Load_{REG}$	Load Regulation	1 mA ≤ I_{OUT} ≤ 300 mA, V_{IN} = V_{OUT} + 2 V T_A = + 25°C			40	mV
I_{LMT}	Current Limit	V_{IN} = V_{OUT} + 2 V	300	500		mA
I_{SHORT}	Short Current Limit	V_{IN} = V_{OUT} + 2 V		100		
I_Q	Quiescent Current	I_{OUT} = 0 mA		50	80	μA
I_{Q_OFF}	Standby Current	V_{EN} = 0 V, T_A = 25°C		0.1	1	μA
V_{ENH}	EN Pin Threshold Voltage	EN Input Voltage “H”	1.0			V
V_{ENL}	EN Pin Threshold Voltage	EN Input Voltage “L”			0.4	V
I_{EN}	EN Pin Current	V_{EN} = 0 to 24 V		1		μA
PSRR	Power Supply Rejection Ratio	V_{IN} = V_{OUT} + 2 V, I_{OUT} = 20 mA, f = 1 kHz		90		dB
e_N	Output Noise Voltage	V_{IN} = V_{OUT} + 2 V, I_{OUT} = 1 mA, f = 10 Hz to 100 kHz, V_{OUT} = 3.3 V, C_{OUT} = 1 μF(5)		70		μV_{RMS}
R_{dis}	Output discharge FET R_{DSON}	V_{EN} < V_{IL} (output disable)		100		Ω
T_{SD}	Thermal Shutdown Temperature	Temperature Increasing from T_A = +25°C(5)		155		℃
T_{SDH}	Thermal Shutdown Hysteresis	Temperature Falling from TSD(5)		25		℃

NOTES:

3. Here V_{IN} means internal circuit can work normal. If V_{IN} < V_{OUT}, Output voltage follow V_{IN} (I_{OUT} = 1 mA), circuit is safety.

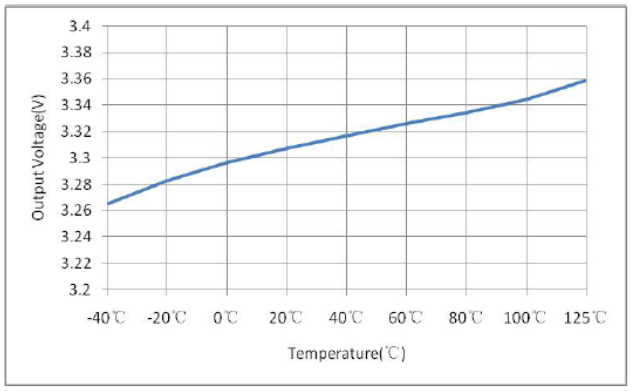
4. V_{DROP} FT test method: test the V_{OUT} voltage at V_{SET} + $V_{DROPMAX}$ with 300 mA output current.

5. Guaranteed by design and characterization. not a FT item.

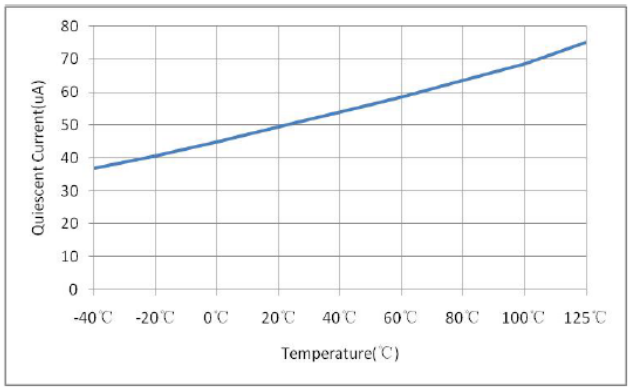
6. The minimum operating voltage is 3 V. V_{DROP} = $V_{IN(MIN)}$ - V_{OUT}.

TYPICAL CHARACTERISTICS

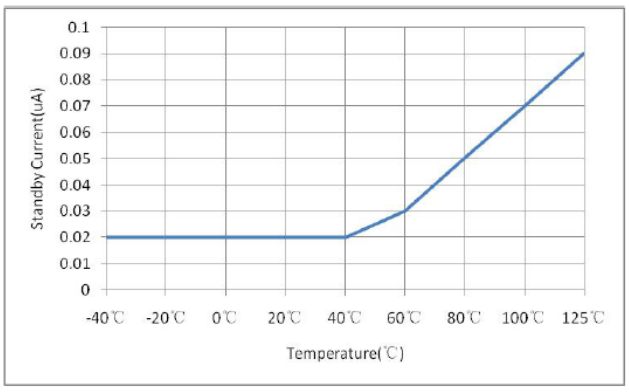
Voltage set 3.3 V (V_{IN} = V_{OUT} + 2 V, I_{OUT} = 10 mA, R1 = 200 kΩ, R2 = 200 kΩ, C_{IN} = C_{OUT} = 1.0 μF, unless otherwise noted. Typical values are at T_A = +25°C).



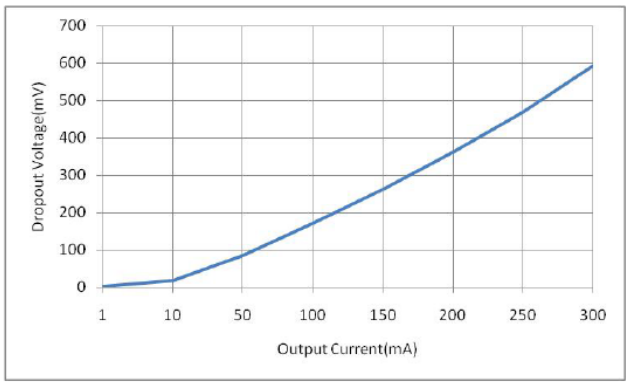
Output Voltage vs. Temperature



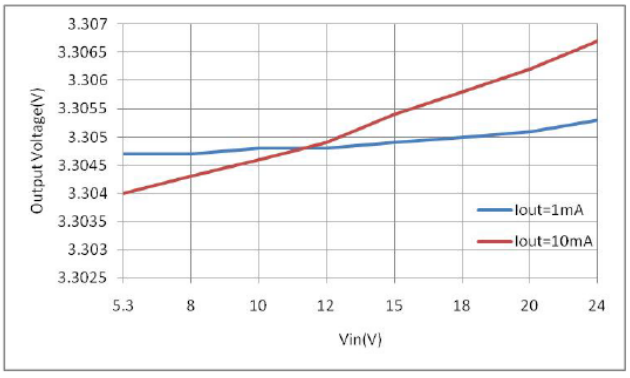
Quiescent Current vs. Temperature



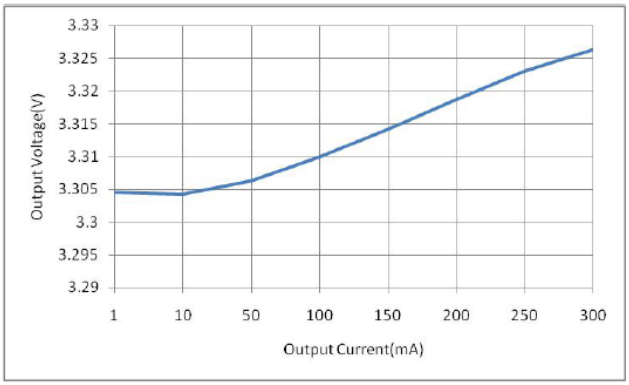
Standby Current vs. Temperature



Dropout Voltage vs Output Current

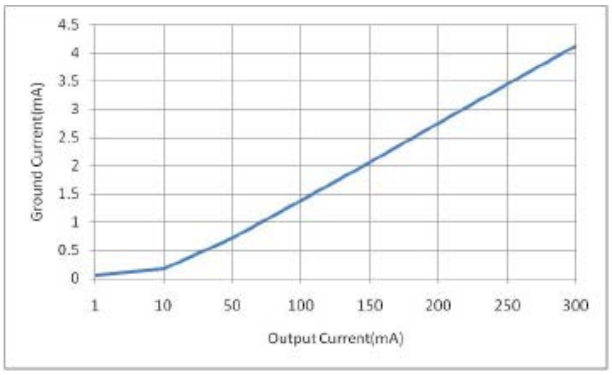


Output Voltage vs. Input Voltage

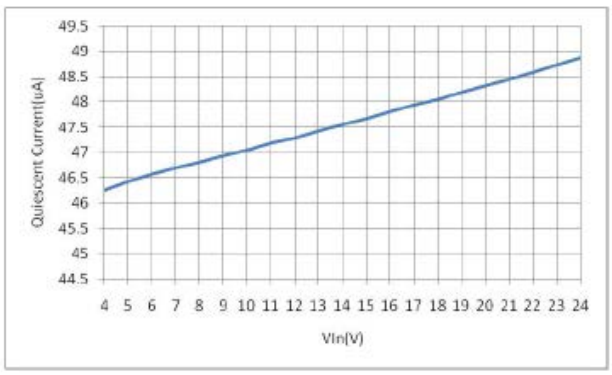


Output Voltage vs. Output Current

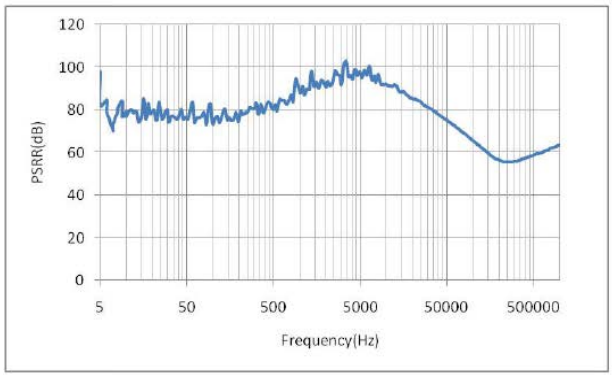
TYPICAL CHARACTERISTICS (Continued)



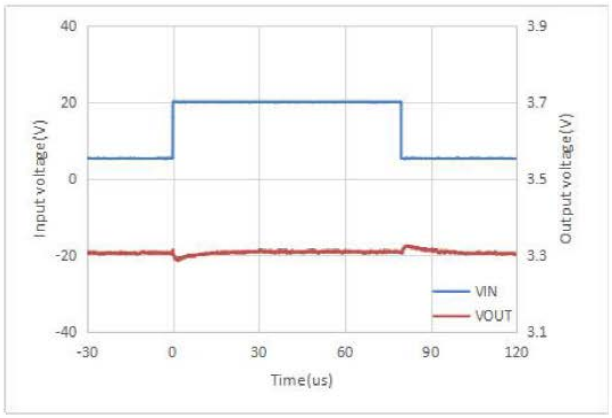
Ground Current vs. Output Current



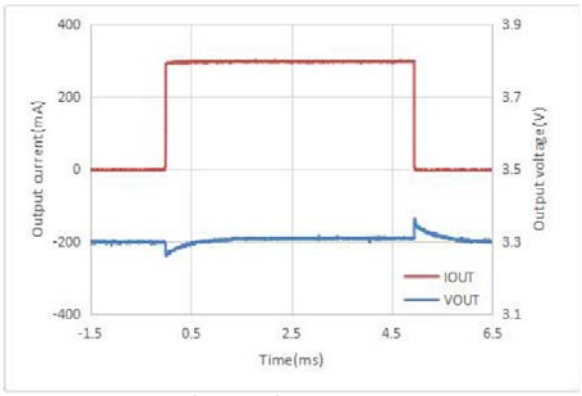
Quiescent Current vs. Input Voltage



PSRR

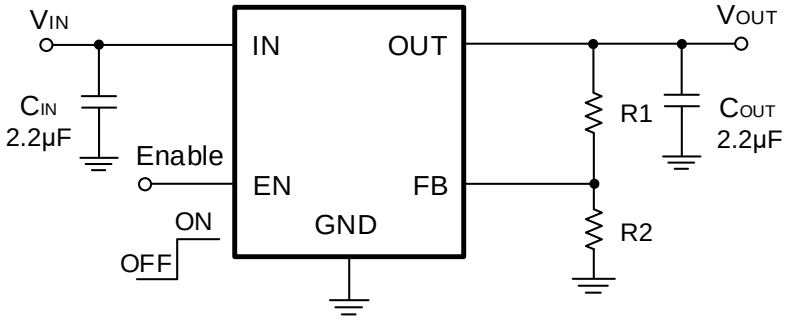


Line-Transient Response(I_{out} = 20 mA)



Load-Transient Response

APPLICATION CIRCUITS

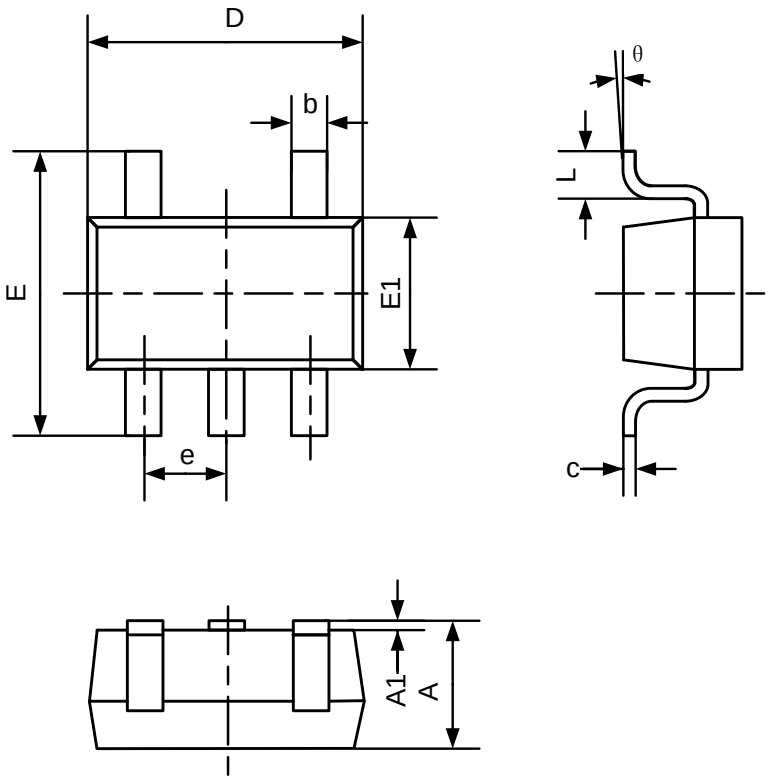


NOTE:

1. V_{OUT} = 0.6 V * (R1 + R2) / R2
2. Recommended R2 = 100 K ~ 1 M

PACKAGE OUTLINE

SOT23-5



Symbol	Dimensions In Millimeters	
	Min	Max
A	1.050	1.250
A1	0.000	0.100
b	0.350	0.500
c	0.100	0.200
D	2.820	3.020
E	2.650	3.050
E1	1.500	1.700
e	0.950BSC	
L	0.300	0.600
θ	0°	8°