High Voltage, Low Power LDO

DESCRIPTION

The SUM3573 is a high voltage, low power consumption and high performance LDO. The family uses an advanced CMOS process and a PMOSFET pass device to achieve fast start-up, with high output voltage accuracy. The SUM3573 is stable with a 1.0 μF ~ 10 μF ceramic output capacitor, and uses a precision voltage reference and feedback loop to achieve a worst-case accuracy of 2% over all load, line, process, and temperature variations.

FEATURES

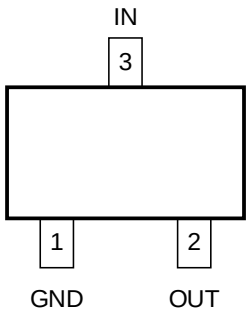
- Wide Input Voltage Range: up to 26 V
- Output Current: 350 mA
- Standard Fixed Output Voltage Options: 1.2 V, 1.8 V, 2.5 V, 3.3 V, 3.6 V and 5.0 V
- Other Output Voltage Options Available on Request
- Low I_Q: 2.5 μA
- Low Dropout Voltage
- Short current protection: 150 mA
- Excellent Load/Line Transient Response
- Line Regulation: 0.01%/V typical
- Package: SOT23-3, SOT23-5, SOT89-3, SOT89-3 (L-Type)

ORDER INFORMATION

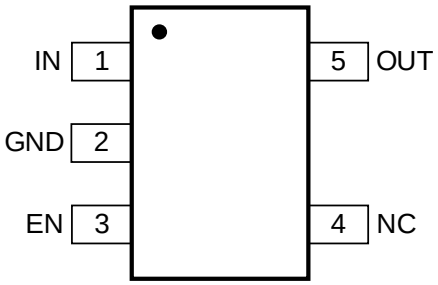
Model	Package	Ordering Number	Packing Option
SUM3573	SOT23-3	SUM3573-XXKA3	Tape and Reel, 3000
	SOT23-5	SUM3573-XXKA5	Tape and Reel, 3000
	SOT89-3	SUM3573-XXP	Tape and Reel, 1000
	SOT89-3 (L-Type)	SUM3573-XXPL	Tape and Reel, 1000

*XX: When expressed as 12, the output voltage is 1.2 V; when expressed as 33 the output voltage is 3.3 V.

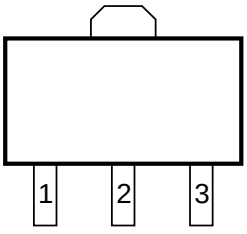
PIN CONFIGURATION (Top View)



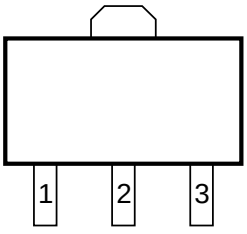
SOT23-3



SOT23-5



SOT89-3

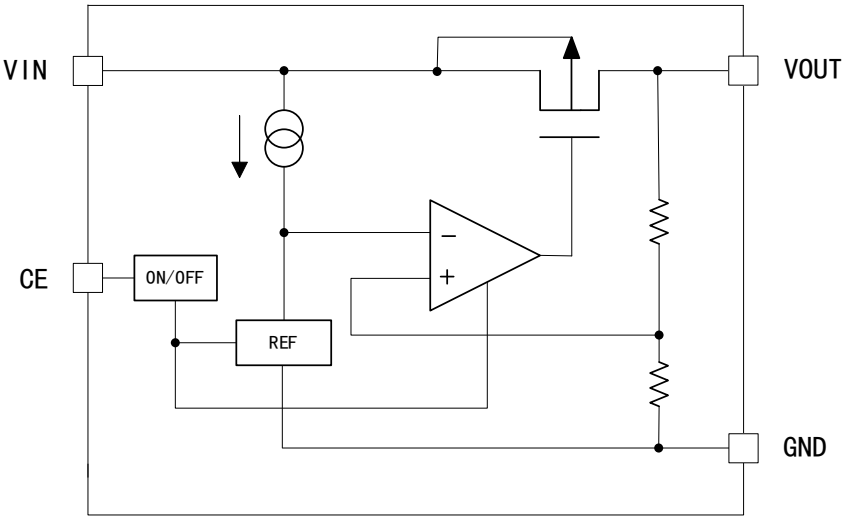


SOT89-3 (L-Type)

PIN DESCRIPTIONS

Pin				Symbol	Description
SOT23-3	SOT23-5	SOT89-3	SOT89-3 (L-Type)		
3	1	2	3	IN	Supply input pin. Must be closely decoupled to GND with a 1 μF or greater ceramic capacitor.
1	2	1	2	GND	Ground.
/	3	/	/	EN	Enable control input, active high.
/	4	/	/	NC	No connection.
2	5	3	1	OUT	Output pin. Bypass a 1 μF ceramic capacitor from this pin to ground.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Input Capacitor

A 1 μF ~ 10 μF ceramic capacitor is recommended to connect between V_{IN} and GND pins to decouple input power supply glitch and noise. The amount of the capacitance may be increased without limit. This input capacitor must be located as close as possible to the device to assure input stability and less noise. For PCB layout, a wide copper trace is required for both V_{IN} and GND.

Output Capacitor

An output capacitor is required for the stability of the LDO. The recommended output capacitance is from 1 μF to 10 μF, Equivalent Series Resistance (ESR) is from 5 mΩ to 100 mΩ, and temperature characteristics are X7R or X5R. Higher capacitance values help to improve load/line transient response. The output capacitance may be increased to keep low undershoot/overshoot. Place output capacitor as close as possible to OUT and GND pins.

Low Quiescent Current

The SUM3573, consuming only around 2.5 μA for all input range and output loading, provides great power saving in portable and low power applications.

Short Current Limit Protection

When output current at the OUT pin is higher than current limit threshold or the OUT pin is short-circuit to GND, the short current limit protection will be triggered and clamp the output current to approximately 100 mA to prevent over-current and to protect the regulator from damage due to overheating.

RECOMMENDED OPERATING CONDITIONS

Parameter	Rating	Unit
Operating Temperature Range	-40 to +85	℃

ABSOLUTE MAXIMUM RATINGS(1)

Parameter	Rating		Unit
IN pin to GND pin	-0.3 to 30		V
OUT pin to GND pin	-0.3 to 6		V
Thermal Resistance (Junction to Ambient)(2)	SOT23-3	360	°C/W
	SOT23-5	250	
	SOT89-3	135	
Power Dissipation @ 25℃	400		mW
Junction Temperature	150		℃
Storage Temperature	-65 to 150		℃
ESD (HBM mode), ESDA/JEDEC JS-001-2017	±2000		V

NOTE:

1) Stresses beyond those listed under “ABSOLUTE MAXIMUM RATINGS” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2) This particular frame decreases the total thermal resistance of the package and increases its ability to dissipate power when an appropriate area of copper on the printed circuit board is available for heat-sinking.

CAUTION

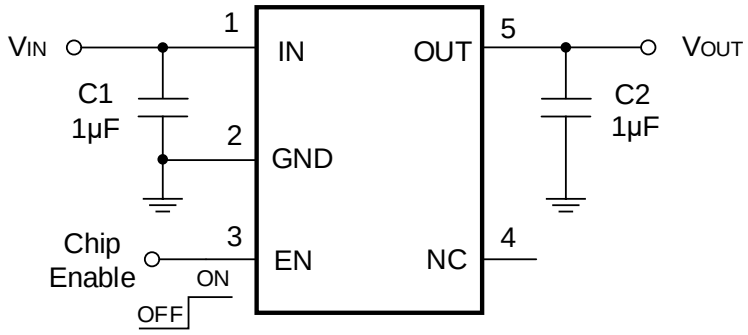
This integrated circuit can be damaged by ESD if you don’t pay attention to ESD protection. SUMSEMI recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications. SUMSEMI reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time. Please contact SUMSEMI sales office to get the latest datasheet.

ELECTRICAL CHARACTERISTICS

V_{IN} = V_{OUT} + 2 V; I_{OUT} = 10 mA, C_{IN} = C_{OUT} = 1.0 μF, unless otherwise noted. Typical values are at T_A = +25°C.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Operating Input Voltage	V_{IN}				26	V
Line Regulation	Reg_{LINE}	V_{IN} ≤ 28 V, I_{OUT} = 10 mA		0.01	0.04	%/V
Dropout Voltage	V_{DROP}	V_{OUT} = 3.0 V, I_{OUT} = 100 mA		330		mV
		V_{OUT} = 3.0 V, I_{OUT} = 200 mA		690		
Load Regulation	Reg_{LOAD}	1 mA ≤ I_{OUT} ≤ 300 mA, V_{IN} = V_{OUT} + 2 V			40	mV
Maximum Output Current	I_{OUT}	V_{IN} = V_{OUT} + 1 V	350			mA
Quiescent Current	I_Q	I_{OUT} = 0 mA		2.5	4	μA
Standby Current	I_{Q_OFF}	V_{EN} = 0 V, T_A = 25°C		0.1	1	μA
EN Pin Threshold Voltage	V_{ENH}	EN Input Voltage “H”	1.2			V
EN Pin Threshold Voltage	V_{ENL}	EN Input Voltage “L”			0.4	V
EN Pin Current	I_{EN}	V_{EN} = 0 V to 28 V		1		μA
Power Supply Rejection Ratio	PSRR	V_{IN} = V_{OUT} + 1 V, I_{OUT} = 20 mA, f = 1 kHz		60		dB
Output Noise Voltage	e_N	V_{IN} = V_{OUT} + 2 V, I_{OUT} = 1 mA, f = 10 Hz to 100 kHz, V_{OUT} = 3 V, C_{OUT} = 1 μF		100		μV_{RMS}
Thermal Shutdown Temperature	T_{SD}	Temperature Increasing from T_A = +25°C		155		°C
Thermal Shutdown Hysteresis	T_{SDH}	Temperature Falling from T_{SD}		20		°C

APPLICATION CIRCUITS



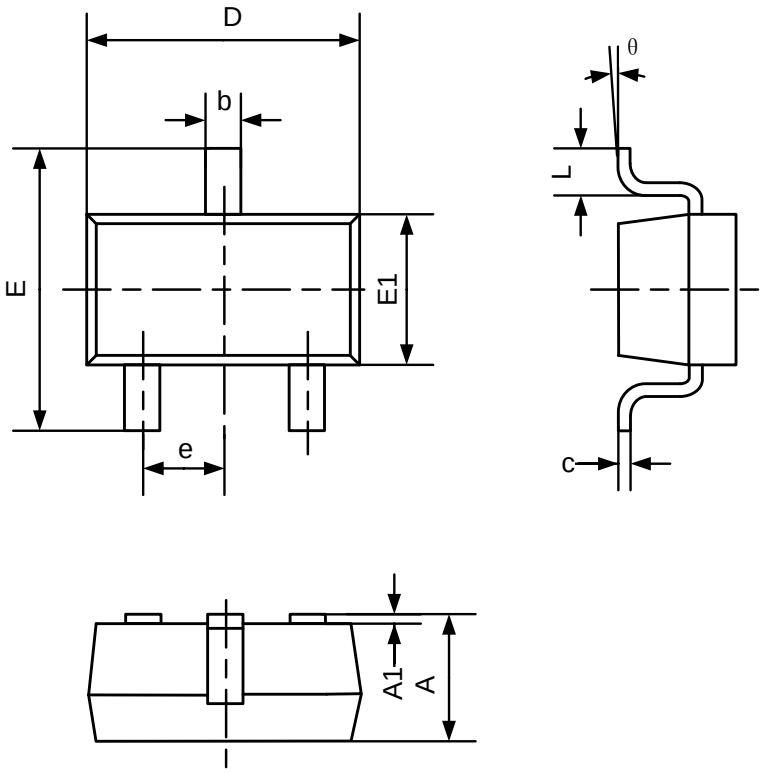
APPLICATION NOTES

1. The Input voltage is the primary electricity (mechanical switch or interface connection). There is contact instantaneous jitter V_{IN} switch for many times, which may cause a large output overshoot (especially when V_{OUT} is no-load), Increasing the output load or changing the input capacitance to ECAP can reduce the output overshoot amplitude.

2. The Input voltage is the secondary electricity. When the V_{IN} is larger than V_{OUT} and smaller than V_{OUT} for a large number of times, the output pin also has an organic rate overshoot. Increasing the output load can reduce the overshoot.

PACKAGE OUTLINE

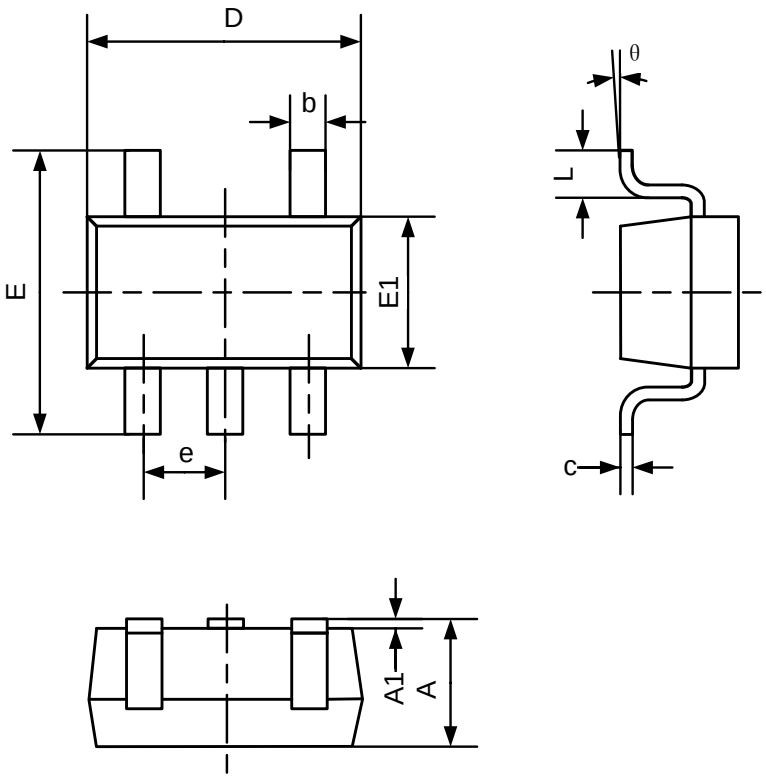
SOT23-3



Symbol	Dimensions In Millimeters	
	Min	Max
A	1.050	1.250
A1	0.000	0.100
b	0.300	0.500
c	0.100	0.200
D	2.820	3.020
E	2.650	2.950
E1	1.500	1.700
e	0.950BSC	
L	0.300	0.600
θ	0°	8°

PACKAGE OUTLINE

SOT23-5



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E	2.650	2.950
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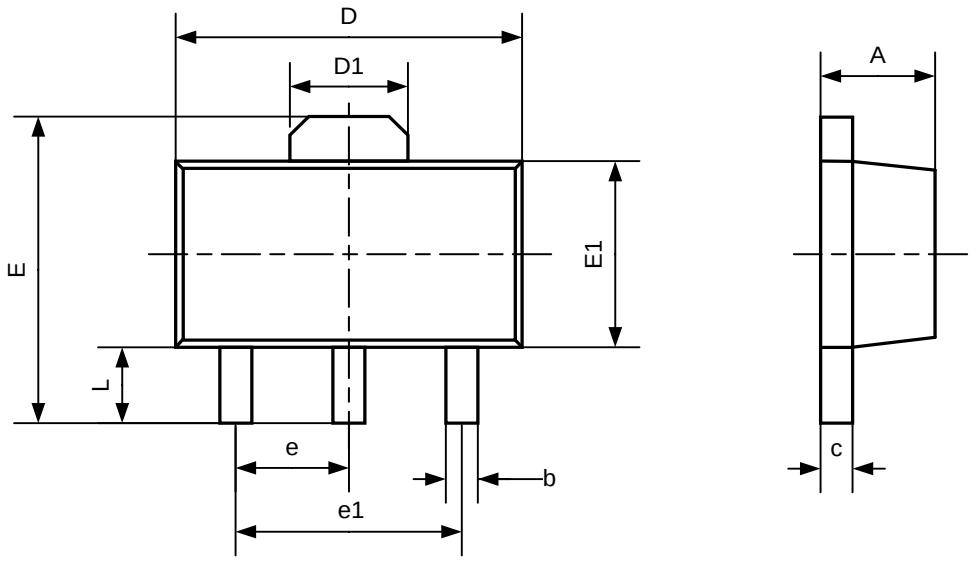
PACKAGE OUTLINE

SOT89-3



Symbol	Dimensions In Millimeters	
	Min	Max
A	1.400	1.600
b	0.320	0.520
c	0.350	0.440
D	4.400	4.600
D1	1.550REF	
E	3.940	4.250
E1	2.300	2.600
e	1.500BSC	
e1	3.000BSC	
L	0.900	1.200