High Voltage, High PSRR Low Noise LDO

DESCRIPTION

The SUM3577 family of low-dropout (LDO), low-power linear regulators offers very high power supply rejection ratio (PSRR) while maintaining very low 40 μA ground current, suitable for RF applications. The family uses an advanced CMOS process and a PMOSFET pass device to achieve fast start-up, very low noise, excellent transient response, and excellent PSRR performance. The SUM3577 is stable with a 1.0 μF ceramic output capacitor, and uses a precision voltage reference and feedback loop to achieve a worst-case accuracy of 2% over all load, line, process, and temperature variations. It is offered in DFN1.0×1.0-4, SOT23-3, SOT23-5 and SOT89-3(L-Type) packages.

FEATURES

- Operating Voltage Range from 1.8 V to 10 V
- Standard Fixed Output Voltage Options : 1.2 V, 1.5 V, 1.8 V, 2.5 V, 2.8 V, 3.0 V, 3.3 V, 3.6 V, 5.0 V
- Output Accuracy: ±2%
- Low Quiescent Current: 40 μA
- Low Dropout Voltage: 120 mV@100 mA/3.3 V
- High PSRR: 80 dB@1 KHz, 10 mA
- Output Current: 500 mA
- Excellent Line and Load Regulation
- Over-Temperature Protection
- Current Limiting Protection
- Output Short-Circuit Protection
- Package: DFN1.0×1.0-4, SOT23-3, SOT23-5, SOT89-3(L-Type)

APPLICATIONS

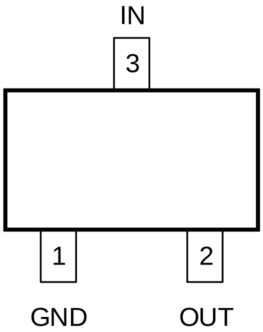
- Battery-Powered Devices
- Reference Voltage Sources
- Other Low Voltage Power Suppliers

ORDER INFORMATION

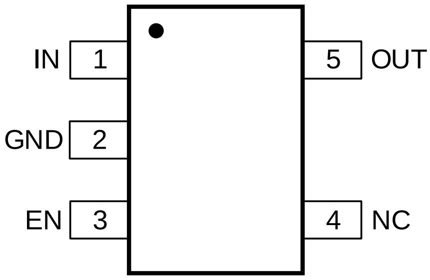
Model	Package	Ordering Number	Packing Option
SUM3577	SOT23-3	SUM3577-XXKA3	Tape and Reel, 3000
	SOT23-5	SUM3577-XXKA5	Tape and Reel, 3000
	DFN1.0 × 1.0-4	SUM3577-XXYB	Tape and Reel, 10000
	SOT89-3(L-Type)	SUM3577-XXPL	Tape and Reel, 1000

*XX: When expressed as 33, the output voltage is 3.3 V.

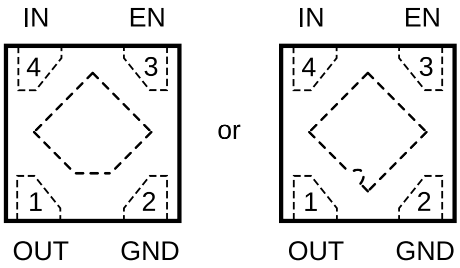
PIN CONFIGURATION



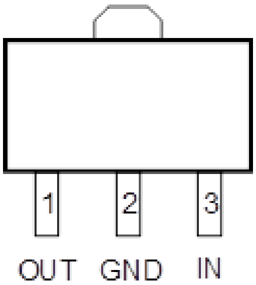
SOT23-3



SOT23-5



DFN1.0 × 1.0-4

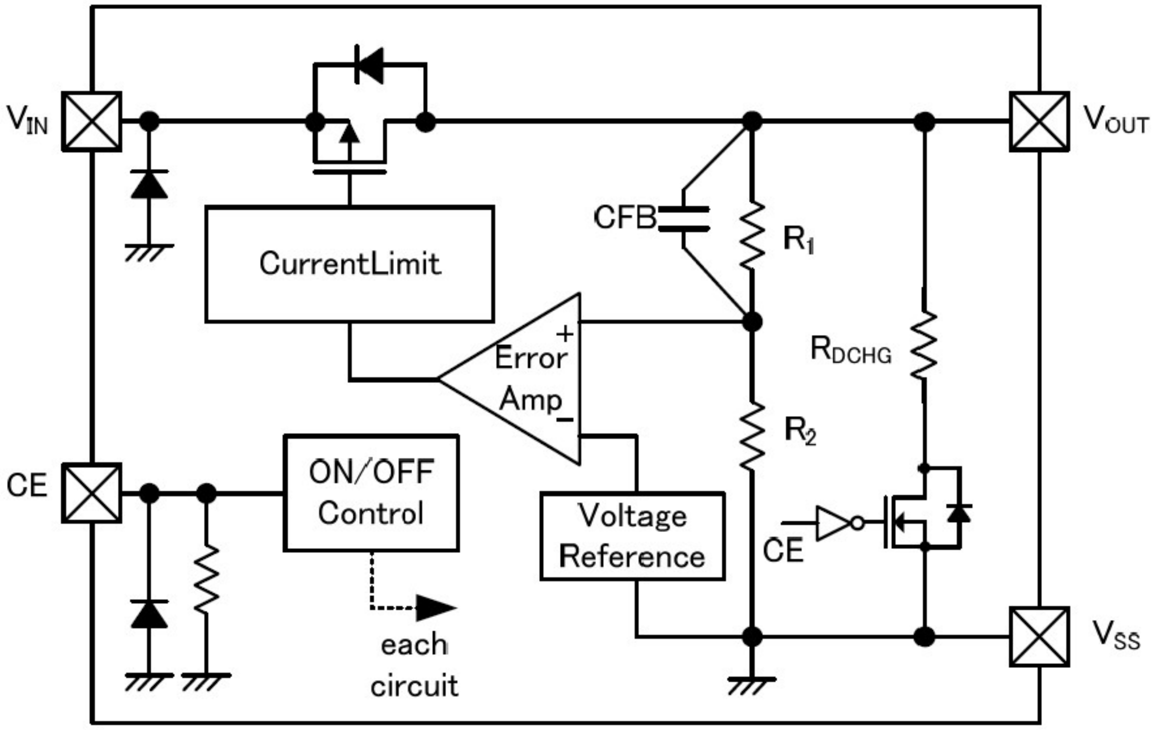


SOT89-3 (L-Type)

PIN FUNCTION

Pin No.				Pin Name	Pin Function
SOT23-5	**SOT23-3**	**DFN1.0 x 1.0-4**	**SOT89-3 (L-Type)**		
1	3	4	3	IN	Supply input pin.
2	1	2	2	GND	Ground.
3		3		EN	Enable control input.
4				NC	No connection.
5	2	1	1	OUT	Output pin.

BLOCK DIAGRAM



DETAIL OPERATION DESCRIPTION

The SUM3577 Series is a low noise, high PSRR, low drop-out voltage regulator. It consists of a current limiter circuit, a driver transistor, a precision voltage reference and an error correction c circuit, and is compatible with low ESR ceramic capacitors. The current limiter's fold-back circuit operates as a short circuit protection as well as the output current limiter.

Current Limiting and Short-Circuit Protection

The current limit circuitry prevents damage to the MOSFET switch and the hub downstream port but can deliver load current up to the current limit threshold of typically 500 mA through the switch. When a heavy load or short circuit is applied to an enabled switch, a large transient current may flow until the current limit circuitry responds. Once this current limit threshold is exceeded the device enters constant current mode until the thermal shutdown occurs or the fault is removed.

ABSOLUTE MAXIMUM RATINGS (1)

Parameter		Rating	Unit
IN Voltage		-0.3 to 12	V
EN Voltage		-0.3 to 12	V
V_{OUT} Pin Voltage		-0.3 to V_{IN}+ 0.3	V
Package Thermal Resistance (2)	SOT23-3	360	℃ /W
	SOT23-5	250	
	DFN1.0 x 1.0-4	280	
	SOT89-3 (L-Type)	135	
Operating Ambient Temperature		-40 to 85	℃
Junction Temperature		-40 to 150	℃
Storage Temperature		-65 to +150	℃
Lead Temperature (Soldering, 10 sec)		260	℃
ESD Susceptibility, Human-body model (per ANSI/ESDA/JEDEC JS-001)		±2000	V

NOTE:

(1) Stresses beyond those listed under "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(2) This particular frame decreases the total thermal resistance of the package and increases its ability to dissipate power when an appropriate area of copper on the printed circuit board is available for heat-sinking.

CAUTION

This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. SUMSEMI recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications. SUMSEMI reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time. Please contact SUMSEMI sales office to get the latest datasheet.

ELECTRIAL CHARACTERISTICS

(V_{IN}=V_{OUT}+1 V, V_{OUT} =3.3 V, C_{IN} = C_{OUT}= 1 µF, T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions		MIN	TYP	MAX	Units
V_{IN}	Input Voltage					10	V
V_{OUT}	Output Accuracy	I_{OUT}= 1 mA		-2		+2	%
I_{LIM}	Current Limit[1]	V_{IN}= 4.3 V, V_{OUT} = 3.3 V			500		mA
I_Q	Quiescent Current	V_{IN}=V_{EN}=V_{OUT}+1 V, No Load			40	60	µA
I_{SHD}	Shutdown Current	V_{IN}= 10 V, V_{EN}= 0 V				0.1	µA
V_{DROP}	Dropout Voltage[2]	I_{OUT}=100 mA, V_{OUT}= 3.3 V			120		mV
		I_{OUT}= 300 mA, V_{OUT}= 3.3 V			380		
		I_{OUT}= 500 mA, V_{OUT}= 3.3 V			700		
S_{LINE}	Line Regulation	V_{IN}= V_{OUT}+1 V to 10 V, I_{OUT}=1 mA			0.05	0.1	%/V
S_{LOAD}	Load Regulation	1 mA≤ I_{OUT} ≤ 500 mA			0.001	0.01	%/mA
I_{SHORT}	Short Current	V_{OUT}= 0 V			100		mA
V_{ENH}	EN High Voltage	V_{IN}= 1.8 V to 10 V, I_{OUT}= 1 mA		1.5			V
V_{ENL}	EN Low Voltage					0.4	V
T_{STR}	Startup Time	From V_{EN} 'L'→'H' to 95%*V_{OUT}, C_{OUT}=1 µF, No Load			60		µs
PSRR	Power Supply Rejection Ratio	C_{IN}=None, V_{OUT}= 3.3 V, I_{OUT}= 10 mA	f= 217 Hz		81		dB
			f= 1 KHz		80		
			f= 10 KHz		66		
T_{SD}	Thermal Shut Down	Temperature rising			155		℃
△T_{SD}	TSD Hysteresis	Temperature falling			20		℃
$R_{DISCHRG}$	R_{ON} of Discharge MOSFET	V_{EN}=0V			80		Ω

Notes:

1. Guaranteed by design
2. The dropout voltage is defined as V_{IN} - V_{OUT}, when V_{OUT}=95%*$V_{OUT(NOM)}$

ELECTRIAL CHARACTERISTICS

(V_{IN}=V_{OUT}+1 V, V_{OUT} =5.0 V, C_{IN} = C_{OUT}= 1 µF, T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions		MIN	TYP	MAX	Units
V_{IN}	Input Voltage					10	V
V_{OUT}	Output Accuracy	I_{OUT}= 1 mA		-2		+2	%
I_{LIM}	Current Limit(1)	V_{IN}= 4.3 V, V_{OUT} = 5.0 V			500		mA
I_Q	Quiescent Current	V_{IN}=V_{EN}=V_{OUT}+1 V, No Load			40	60	µA
I_{SHD}	Shutdown Current	V_{IN}= 10 V, V_{EN}= 0 V				0.1	µA
V_{DROP}	Dropout Voltage(2)	I_{OUT}=100 mA, V_{OUT}= 5.0 V			114		mV
		I_{OUT}= 300 mA, V_{OUT}= 5.0 V			370		
		I_{OUT}= 500 mA, V_{OUT}= 5.0 V			730		
S_{LINE}	Line Regulation	V_{IN}= V_{OUT}+1 V to 10 V, I_{OUT}=1 mA			0.05	0.1	%/V
S_{LOAD}	Load Regulation	1 mA≤ I_{OUT} ≤ 500 mA			0.001	0.01	%/mA
I_{SHORT}	Short Current	V_{OUT}= 0 V			100		mA
V_{ENH}	EN High Voltage	V_{IN}= 1.8 V to 10 V, I_{OUT}= 1 mA		1.5			V
V_{ENL}	EN Low Voltage					0.4	V
T_{STR}	Startup Time	From V_{EN} 'L'→'H' to 95%*V_{OUT}, C_{OUT}=1 µF, No Load			60		µs
PSRR	Power Supply Rejection Ratio	C_{IN}=None, V_{OUT}= 5.0 V, I_{OUT}= 10 mA	f= 217 Hz		81		dB
			f= 1 KHz		80		
			f= 10 KHz		66		
T_{SD}	Thermal Shut Down	Temperature rising			155		°C
△T_{SD}	TSD Hysteresis	Temperature falling			20		°C
$R_{DISCHRG}$	R_{ON} of Discharge MOSFET	V_{EN}=0 V			80		Ω

Notes:

1. Guaranteed by design
2. The dropout voltage is defined as V_{IN} - V_{OUT}, when V_{OUT}=95%*$V_{OUT(NOM)}$

TYPICAL PERFORMANCE CHARACTERISTIC

（Tested under T_A =25℃, unless otherwise specified）

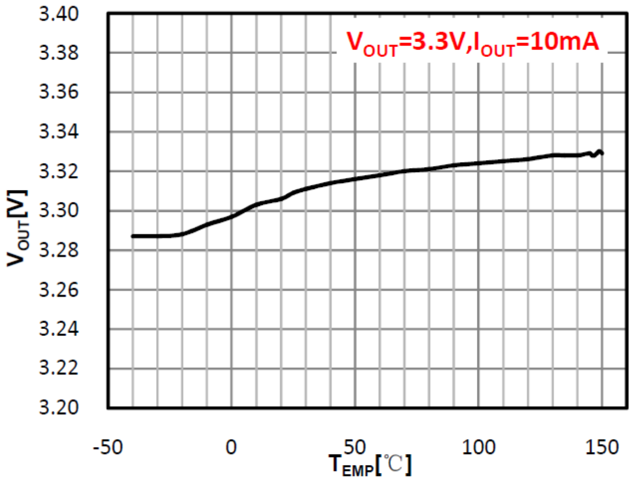


Figure 1. V_{OUT} vs Temperature

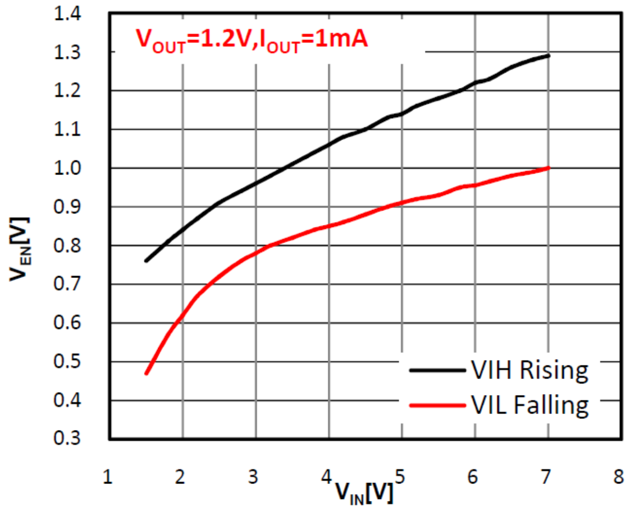


Figure 2. V_{EN} vs V_{IN}

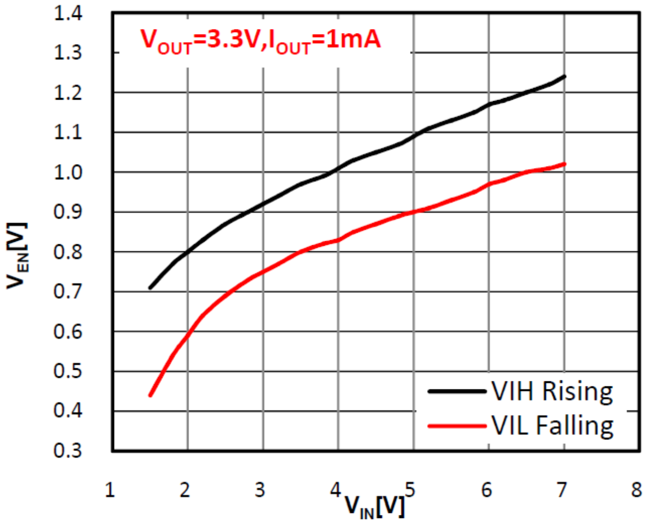


Figure 3. V_{EN} vs V_{IN}

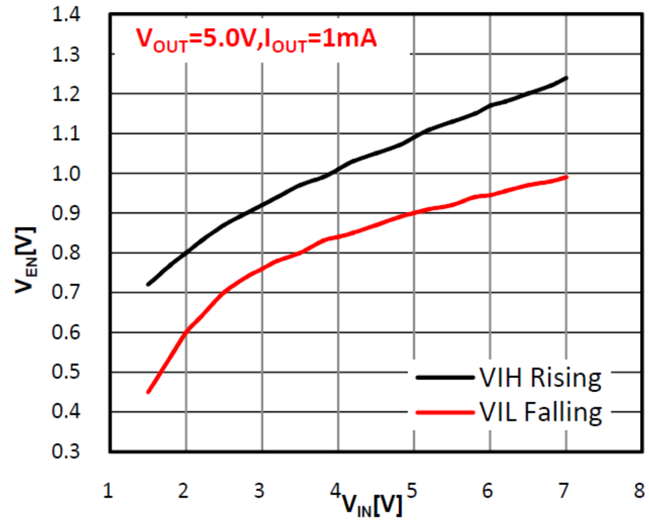


Figure 4. V_{EN} vs V_{IN}

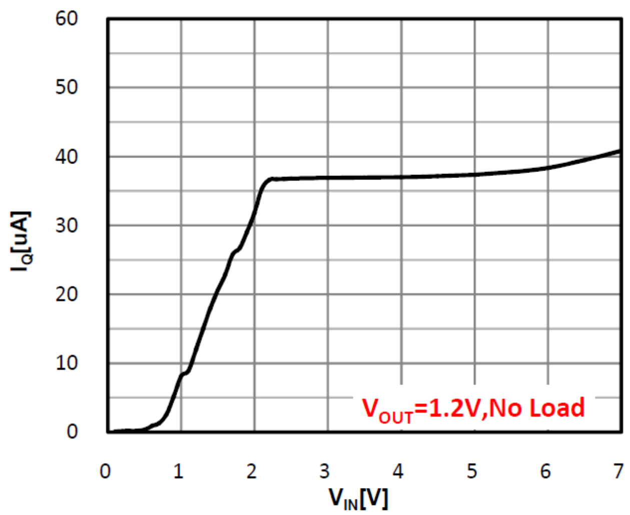


Figure 5. I_Q VS V_{IN}

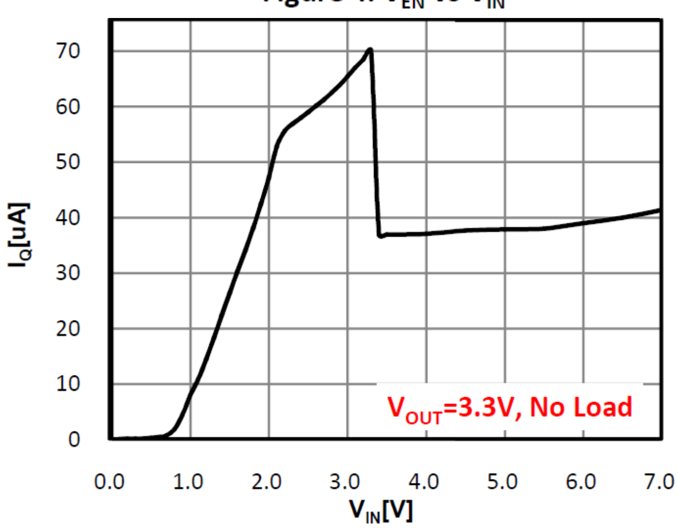


Figure 6. I_Q VS V_{IN}

TYPICAL PERFORMANCE CHARACTERISTIC

（Tested under T_A =25℃, unless otherwise specified）

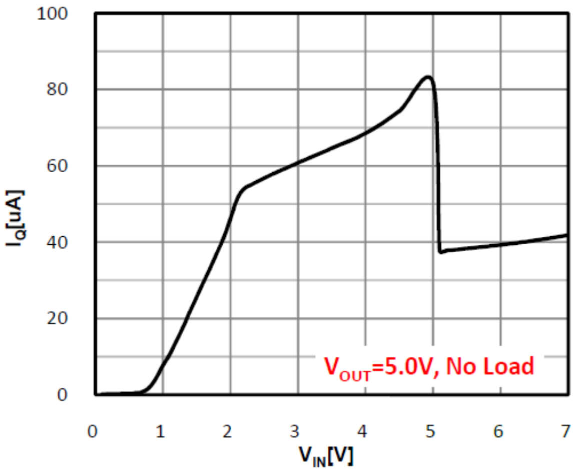


Figure 7. I_Q VS V_{IN}

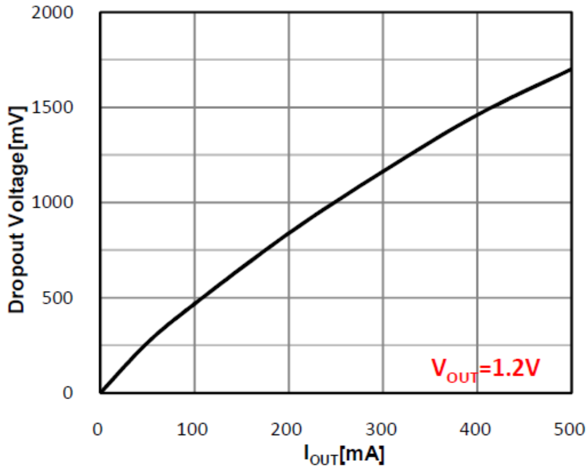


Figure 8. Dropout Voltage VS I_{OUT}

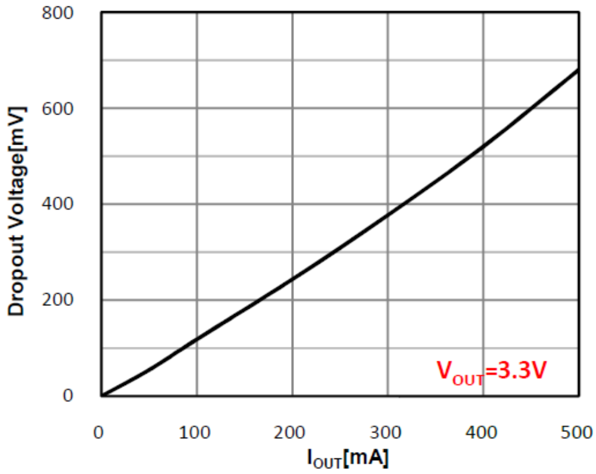


Figure 9. Dropout Voltage VS I_{OUT}

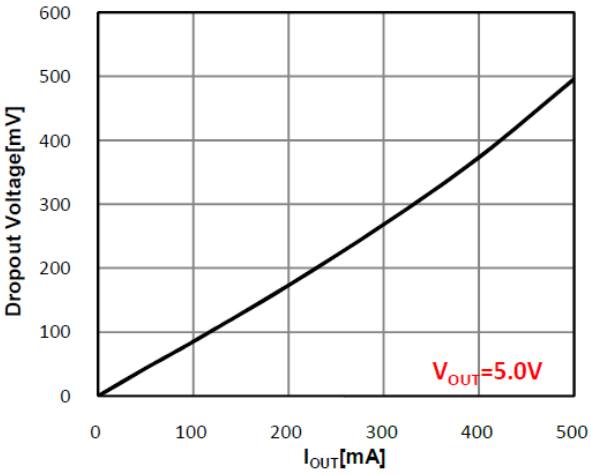


Figure 10. Dropout Voltage VS I_{OUT}

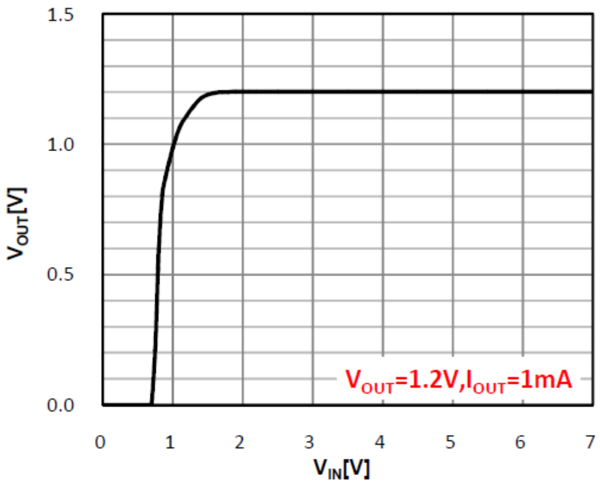


Figure 11. V_{OUT} vs V_{IN}

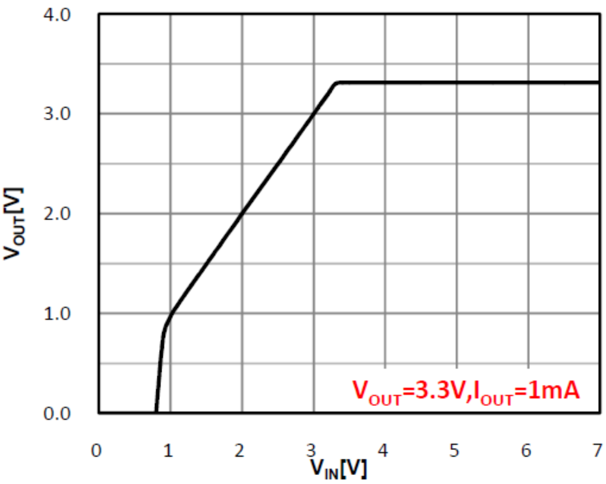


Figure 12. V_{OUT} vs V_{IN}

TYPICAL PERFORMANCE CHARACTERISTIC

（Tested under T_A =25℃, unless otherwise specified）

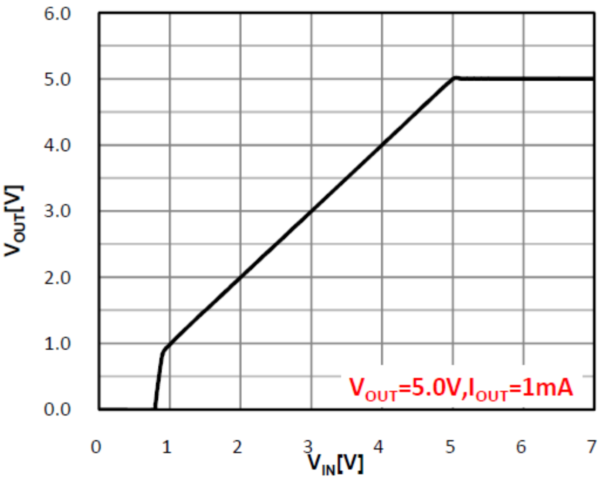


Figure 13. V_{OUT} vs V_{IN}

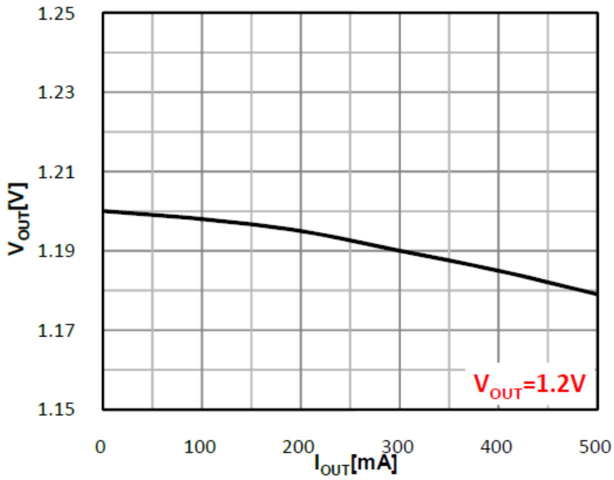


Figure 14. Load Regulation

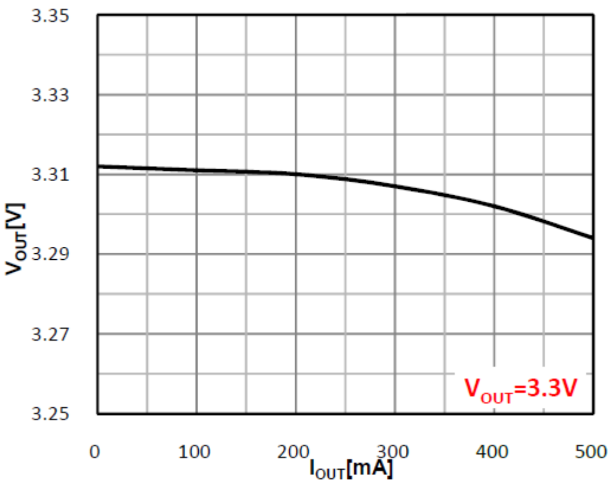


Figure 15. Load Regulation

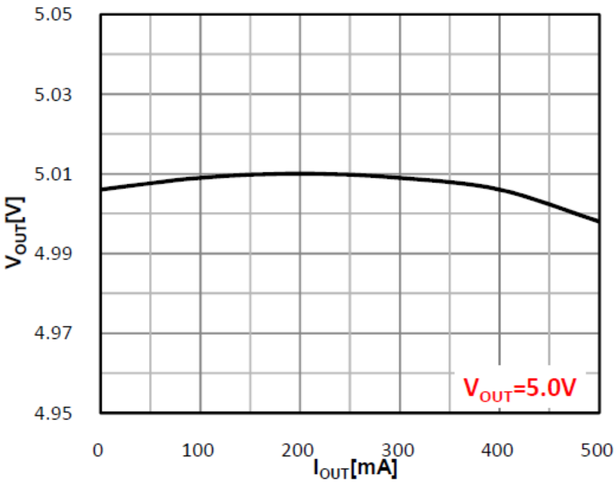
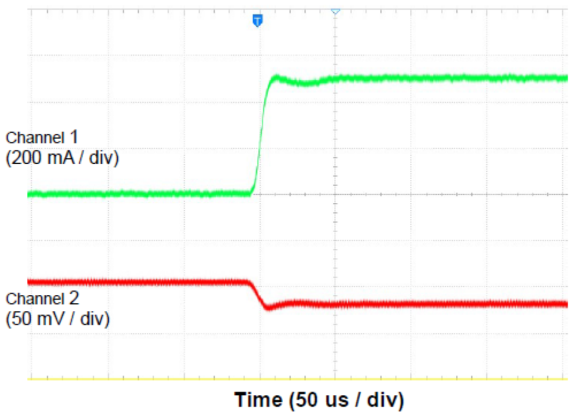
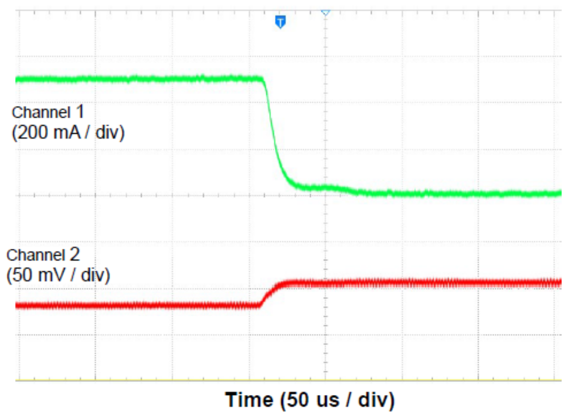


Figure 16. Load Regulation



Channel 1 = I_{OUT}, channel 2 =V_{OUT}, V_{IN}=3.0V, V_{OUT}=1.2V

Figure 17. Load Transient (1 mA to 500 mA)

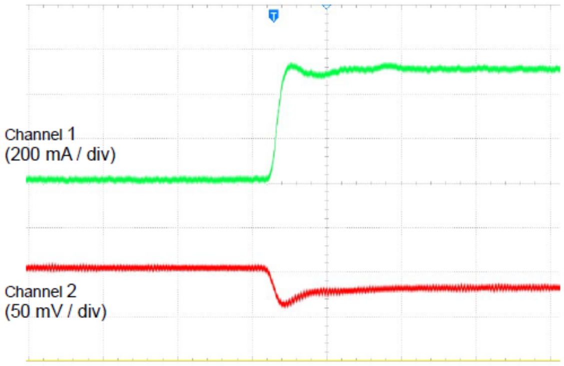


Channel 1 = I_{OUT}, channel 2 =V_{OUT}, V_{IN}=3.0V, V_{OUT}=1.2V

Figure 18. Load Transient (500 mA to 1 mA)

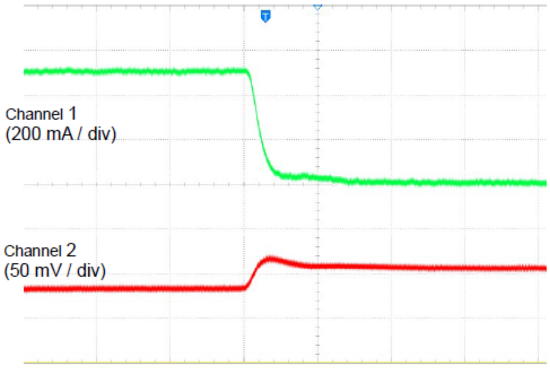
TYPICAL PERFORMANCE CHARACTERISTIC

（Tested under T_A =25℃, unless otherwise specified）



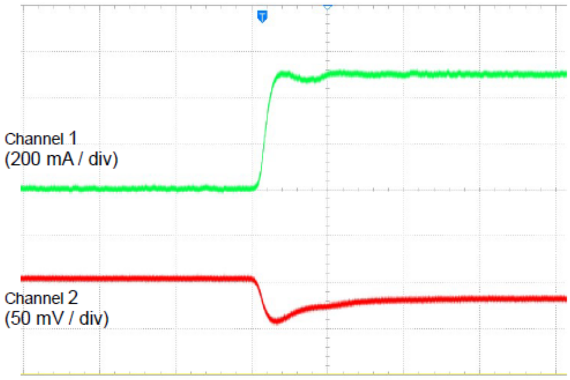
Channel 1 = I_{OUT}, channel 2 =V_{OUT}, V_{IN}=4.3V, V_{OUT}=3.3V

Figure 19. Load Transient (1 mA to 500 mA)



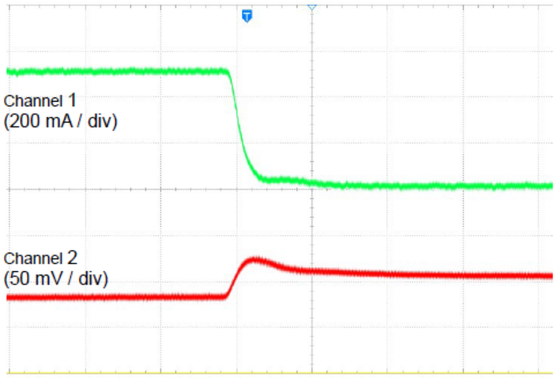
Channel 1 = I_{OUT}, channel 2 =V_{OUT}, V_{IN}=4.3V, V_{OUT}=3.3V

Figure 20. Load Transient (500 mA to 1 mA)



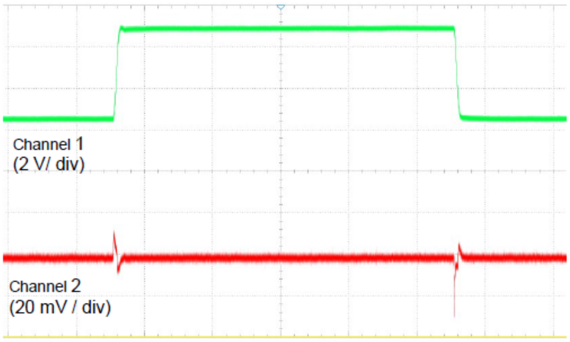
Channel 1 = I_{OUT}, channel 2 =V_{OUT}, V_{IN}=6.0V, V_{OUT}=5.0V

Figure 21. Load Transient (1 mA to 500 mA)



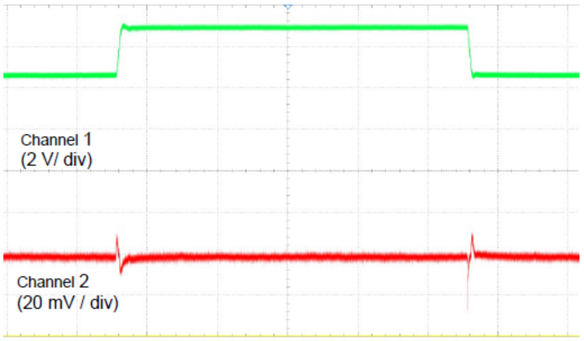
Channel 1 = I_{OUT}, channel 2 =V_{OUT}, V_{IN}=6.0V, V_{OUT}=5.0V

Figure 22. Load Transient (500 mA to 1 mA)



Channel 1 = V_{IN}, channel 2 =V_{OUT}, V_{IN}=2.2V→7.0V, Tr=Tf=5us, V_{OUT}=1.2V, I_{OUT}=10mA

Figure 23. Line Transient

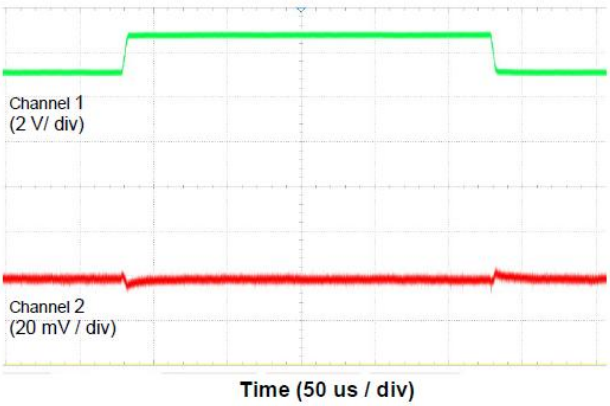


Channel 1 = V_{IN}, channel 2 =V_{OUT}, V_{IN}=4.3V→7.0V, Tr=Tf=5us, V_{OUT}=3.3V, I_{OUT}=10mA

Figure 24. Line Transient

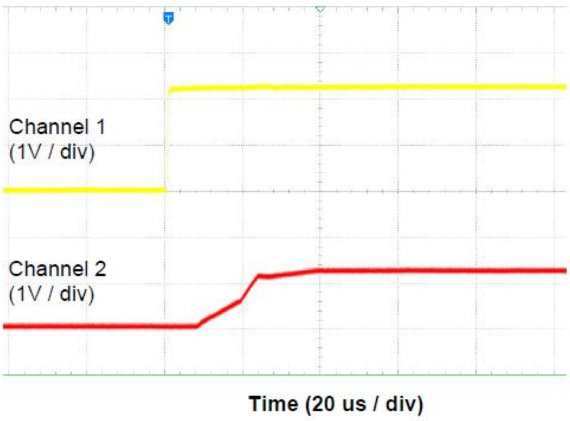
TYPICAL PERFORMANCE CHARACTERISTIC

（Tested under T_A =25℃, unless otherwise specified）



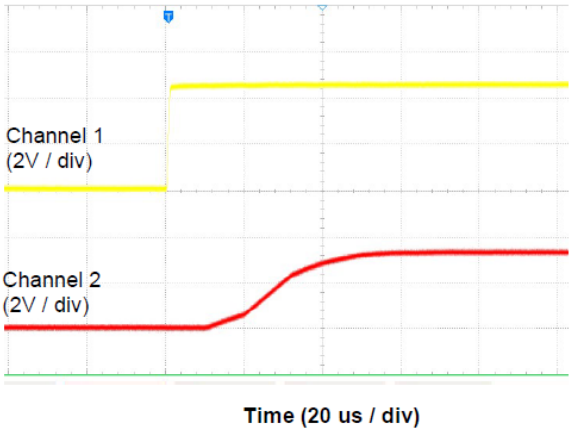
Channel 1 = V_{IN}, channel 2 =V_{OUT}, V_{IN}=5.5V→7.0V, Tr=Tf=5us, V_{OUT}=5.0V, I_{OUT}=10mA

Figure 25. Line Transient



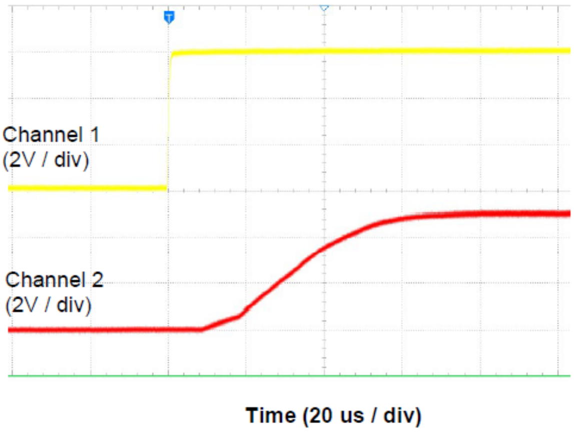
Channel 1 = En, channel 2 =V_{OUT}, V_{OUT}=1.2V, No Load

Figure 26. Power-Up with Enable



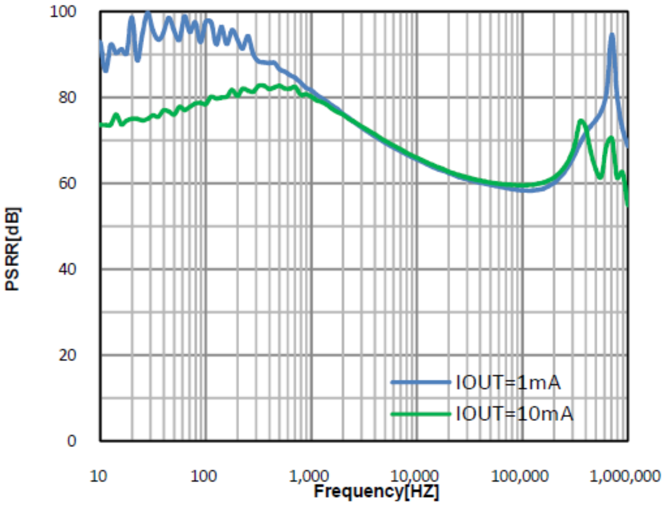
Channel 1 = En, channel 2 =V_{OUT}, V_{OUT}=3.3V, No Load

Figure 27. Power-Up with Enable



Channel 1 = En, channel 2 =V_{OUT}, V_{OUT}=5.0V, No Load

Figure 28. Power-Up with Enable



V_{OUT}=3.3V, V_{IN}=4.3V, V_{PP}=0.2V,C_{IN}=non, C_{OUT}=1uF

Figure 29. PSRR vs Frequency

APPLICATION INFORMATION

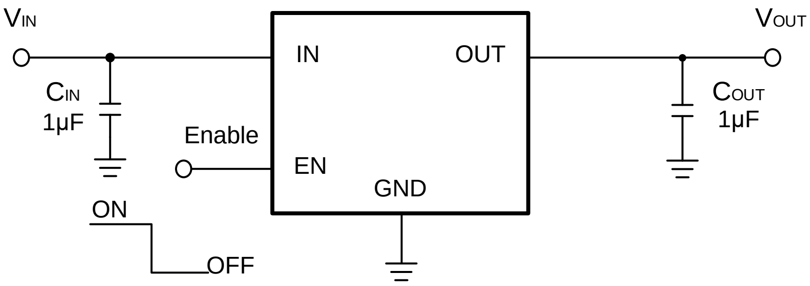
Input Capacitor Selection

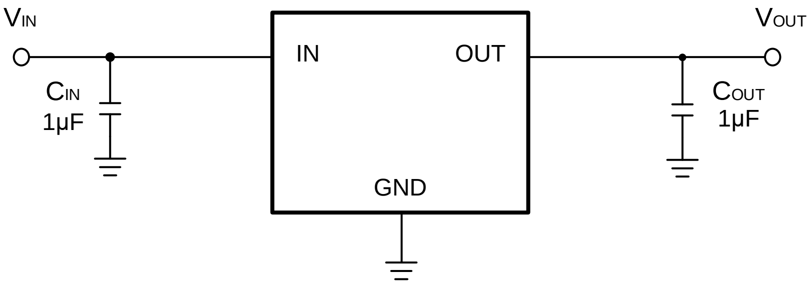
Like any low-dropout regulator, the external capacitors used with the SUM3577 Series must be carefully selected for regulator stability and performance. Using a capacitor whose value is ≥ 1 μF on the SUM3577 Series input and the amount of capacitance can be increased without limit. An at least 10 μF input capacitor is needed if input ripple voltage V_{PP} > 1 V. The input capacitor must be located a distance less than 0.5 inch from the input pin of the IC and returned to a clean analog ground. Any good quality ceramic or tantalum can be used for this capacitor. The capacitor with larger value and lower ESR (equivalent series resistance) provides better PSRR and line-transient response.

Output Capacitor Selection

The output capacitor must meet both requirements for minimum amount of capacitance and ESR in all LDOs application. The SUM3577 Series is designed specifically to work with low ESR ceramic output capacitor in space-saving and performance consideration. Using a ceramic capacitor whose value is at least 1 μF on the SUM3577 Series output ensures stability. An appropriate output capacitor can reduce noise and improve load transient response and PSRR. The output capacitor should be located not more than 0.5 inch from the V_{OUT} pin of the SUM3577 Series and returned to a clean analog ground.

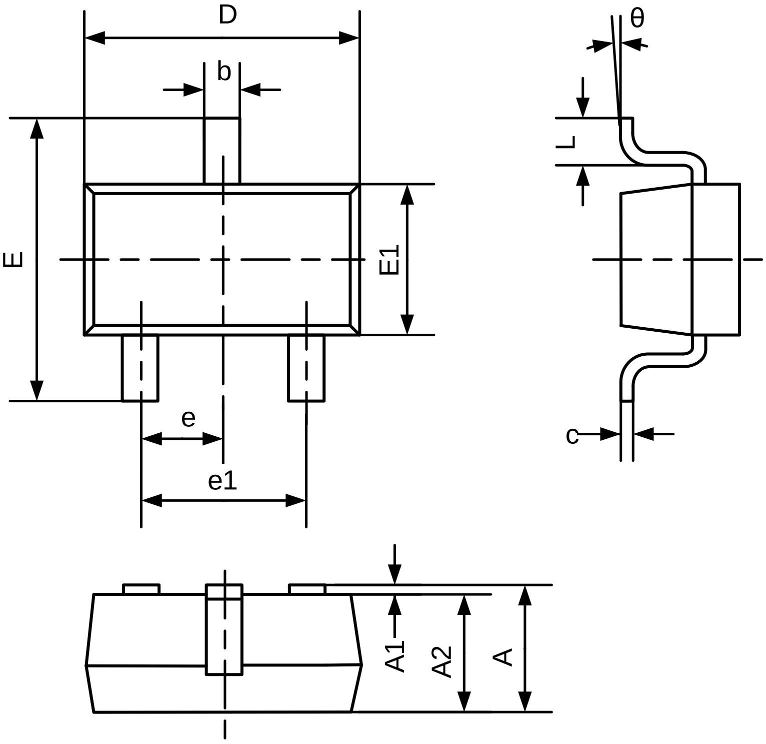
APPLACATION CIRCUITS





PACKAGE DIMENSION

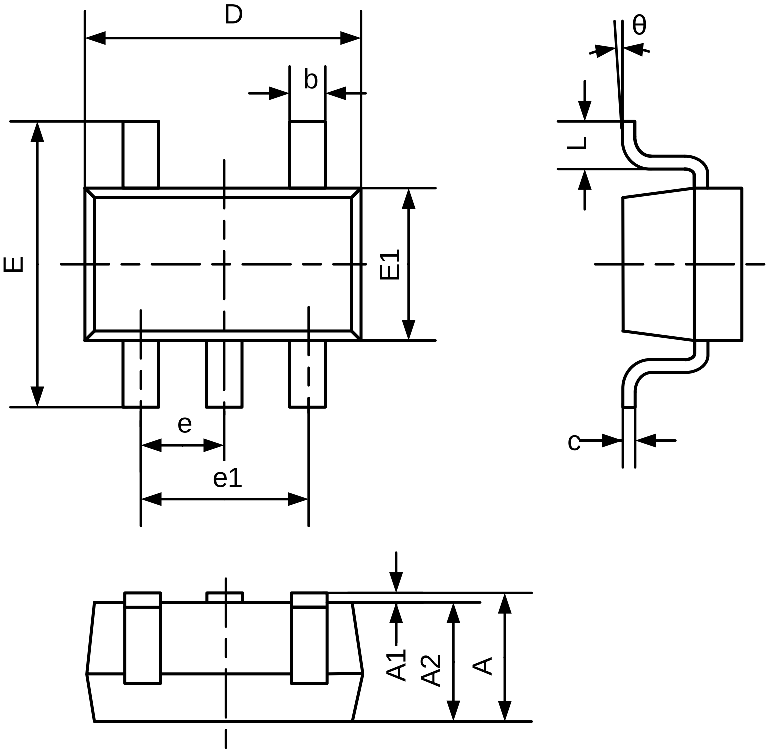
SOT23-3



Symbol	Dimensions In Millimeters	
	MIN	MAX
A	1.050	1.250
A1	0.000	0.100
A2	1.000	1.150
b	0.300	0.400
c	0.100	0.200
D	2.820	3.020
E	2.650	2.950
E1	1.500	1.700
e	0.950BSC	
e1	1.800	2.000
L	0.300	0.600
θ	0°	8°

PACKAGE DIMENSION

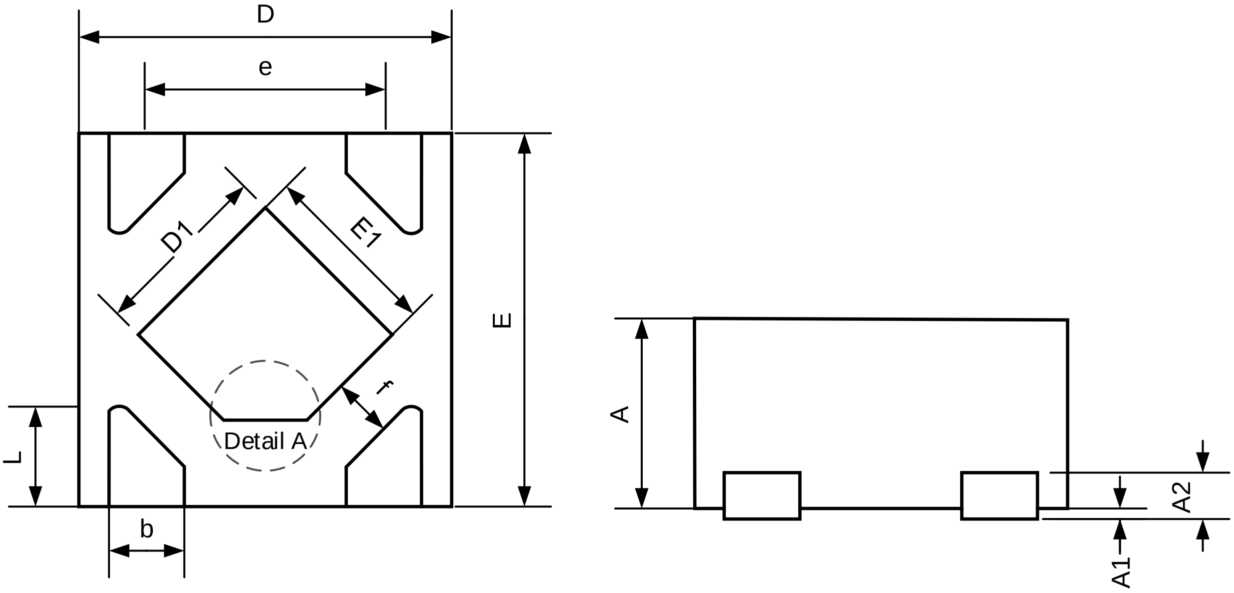
SOT23-5



Symbol	Dimensions In Millimeters	
	MIN	**MAX**
A	0.700	1.250
A1	0.000	0.100
A2	0.700	1.150
b	0.350	0.500
c	0.080	0.200
D	2.820	3.020
E	2.650	2.950
E1	1.500	1.700
e	0.950 BSC	
e1	1.800	2.000
L	0.300	0.600
θ	0°	8°

PACKAGE DIMENSION

DFN1.0 × 1.0-4



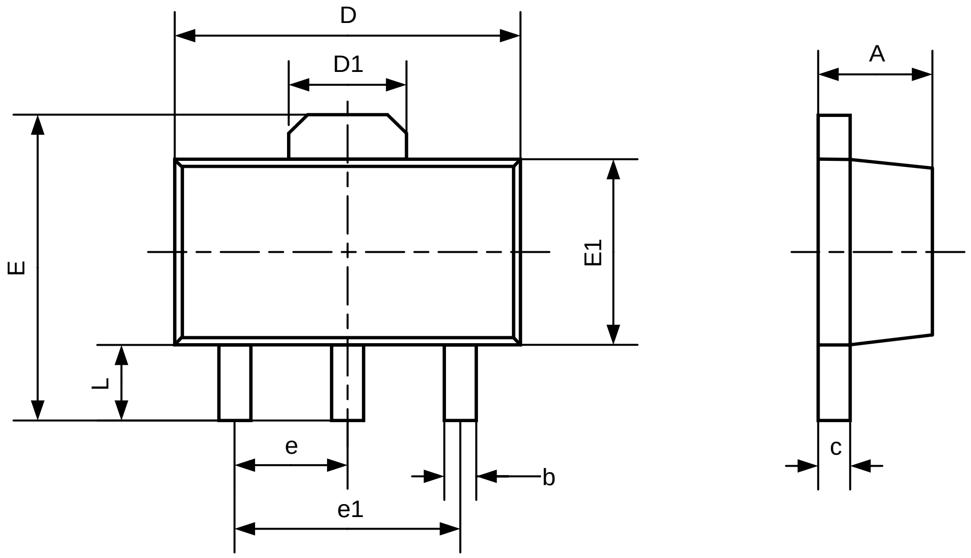
Detail A:

Note: Detail A has two kinds of shapes

Symbol	Dimensions In Millimeters		
	MIN	**MOD**	**MAX**
A	0.400	0.500	0.550
A1	0.000	0.025	0.050
A2	0.125 REF		
D	0.950	1.000	1.050
D1	0.380	0.480	0.580
E	0.950	1.000	1.050
E1	0.380	0.480	0.580
b	0.150	0.200	0.250
e	0.650 BSC		
f	0.190	0.195	0.200
L	0.150	0.250	0.350

PACKAGE DIMENSION

SOT89-3



Symbol	Dimensions In Millimeters	
	Min	**Max**
A	1.400	1.600
b	0.320	0.520
c	0.350	0.440
D	4.400	4.600
D1	1.550REF	
E	3.940	4.250
E1	2.300	2.600
e	1.500BSC	
e1	3.000BSC	
L	0.900	1.200

V 1.5