

High Input Very-Low I_Q 500mA LDO

DESCRIPTION

SUM3584 series are the high input very low I_Q 500 mA LDO with enable function that operates from 3.0 V ~ 18 V, is designed specifically for portable battery-powered applications which require ultra-low quiescent current. The very-low consumption of type 1.0 μ A ensures long battery life and dynamic transient boost feature improves device transient response for wireless communication applications.

SUM3584 series are offered SOT23-5 package.

FEATURES

- Wide Input Voltage Range: 3.0 V ~ 18 V
- Up to 500 mA Load Current
- Very Low I_Q is 1.0 μ A Typical
- Fixed Output Voltage: 3.0 V, 3.3 V, 3.6 V, 5.0 V, etc
- Low Dropout: 765 mV @ 500 mA Load @ $V_{OUT} = 3.3$ V
- Excellent Load/Line Transient Response
- High Ripple Rejection: 60 dB @1 KHz
- Package: SOT23-5

ORDER INFORMATION

Model	Package	Ordering Number	Packing Option
SUM3584	SOT23-5	SUM3584-XXKA5	Tape and Reel, 3000

*XX: when expressed as 30 the output voltage is 3.0 V.

SOT23-5

Pin	Symbol	Description
SOT23-5		
1	IN	Supply input pin.
2	GND	Ground.
3	EN	Enable control input, active high.
4	NC	No connection.
5	OUT	Output pin.

The diagram illustrates a precision current source circuit. The input (IN) is connected to the non-inverting input (+) of an operational amplifier. The inverting input (-) is connected to a reference voltage (REF) and the output of a current limit block. The output of the op-amp drives a MOSFET driver, which in turn drives a MOSFET. The MOSFET's source is connected to ground (GND) through a resistor labeled R_{LOW} . The MOSFET's drain is connected to the output (OUT) and also to a thermal shutdown block. A current limit block is connected between the output (OUT) and the inverting input (-) of the op-amp. An adaptive bias block is connected between the output (OUT) and the non-inverting input (+) of the op-amp. A logic block is connected between the output (OUT) and the inverting input (-) of the op-amp. The output (OUT) is also connected to a resistor network consisting of three resistors in series, with the bottom node connected to GND. The output (OUT) is also connected to a MOSFET driver, which is connected to the MOSFET's gate. The MOSFET's source is connected to GND through a resistor labeled R_{LOW} . The MOSFET's drain is connected to the output (OUT) and also to a thermal shutdown block. A current limit block is connected between the output (OUT) and the inverting input (-) of the op-amp. An adaptive bias block is connected between the output (OUT) and the non-inverting input (+) of the op-amp. A logic block is connected between the output (OUT) and the inverting input (-) of the op-amp. The output (OUT) is also connected to a resistor network consisting of three resistors in series, with the bottom node connected to GND.

FUNCTIONAL DESCRIPTION

Input Capacitor

A 1 μF ~ 10 μF ceramic capacitor is recommended to connect between V_{IN} and GND pins to decouple input power supply glitch and noise. The amount of the capacitance may be increased without limit. This input capacitor must be located as close as possible to the device to assure input stability and less noise. For PCB layout, a wide copper trace is required for both V_{IN} and GND.

Output Capacitor

An output capacitor is required for the stability of the LDO. The recommended output capacitance is from 1 μF to 10 μF , Equivalent Series Resistance (ESR) is from 5 m Ω to 100 m Ω , and temperature characteristics are X7R or X5R. Higher capacitance values help to improve load/line transient response. The output capacitance may be increased to keep low undershoot/overshoot. Place output capacitor as close as possible to V_{OUT} and GND pins.

Enable

The SUM3584 delivers the output power when it is set to enable state. When it works in disable state, there is no output power and the operation quiescent current is almost zero. The enable pin (EN) is active high.

Dropout Voltage

The SUM3584 uses a PMOS pass transistor to achieve low dropout. When ($V_{\text{IN}} - V_{\text{OUT}}$) is less than the dropout voltage (V_{DROP}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{\text{DS(ON)}}$ of the PMOS pass element. V_{DROP} scales approximately with output current because the PMOS device behaves like a resistor in dropout mode. As with any linear regulator, PSRR and transient response degrade as ($V_{\text{IN}} - V_{\text{OUT}}$) approaches dropout operation.

Thermal Shutdown

Thermal shutdown protection disables the output when the junction temperature rises to approximately 160°C. Disabling the device eliminates the power dissipated by the device, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is again enabled.

Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits regulator dissipation, protecting the LDO from damage as a result of overheating. Activating the thermal shutdown feature usually indicates excessive power dissipation as a result of the product of the ($V_{\text{IN}} - V_{\text{OUT}}$) voltage and the load current. For reliable operation, limit junction temperature to 150°C maximum.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula:

$$P_{\text{D(MAX)}} = (T_{\text{J(MAX)}} - T_{\text{A}}) / \theta_{\text{JA}}$$

where $T_{\text{J(MAX)}}$ is the maximum junction temperature, T_{A} is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications the maximum junction temperature is 150°C and T_A is the ambient temperature. The junction to ambient thermal resistance, θ_{JA} is layout dependent.

Current-Limit Protection

The SUM3584 provides current limit function to prevent the device from damages during over-load or shorted-circuit condition. This current is detected by an internal sensing transistor.

Layout Guidelines

- Place input and output capacitors as close to the device as possible.
- Use copper planes for device connections in order to optimize thermal performance.
- Place thermal vias around the device to distribute heat.
- Do not place a thermal via directly beneath the thermal pad. A via can wick solder or solder paste away from the thermal pad joint during the soldering process, leading to a compromised solder joint on the thermal pad.

CAUTION

This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. SUMSEMI recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

SUMSEMI reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time. Please contact SUMSEMI sales office to get the latest datasheet.

RECOMMENDED OPERATING CONDITIONS

Symbol	Item	Rating	Unit
V _{IN}	Input Voltage	3.0 to 18	V
I _{OUT}	Output Current	0 to 500	mA
T _A	Operating Ambient Temperature	-40 to 85	°C
C _{IN}	Effective Input Ceramic Capacitor Value	1 to 10	μF
C _{OUT}	Effective Output Ceramic Capacitor Value	1 to 10	μF
ESR	Input and Output Capacitor Equivalent Series Resistance	5 to 100	mΩ

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Parameter		Rating	Unit
Input Voltage ⁽²⁾		-0.3 to 22	V
Output Voltage		-0.3 to 6	V
Chip Enable Input		-0.3 to 18	V
Junction to Ambient Thermal Resistance (θ _{JA}), ⁽³⁾		SOT23-5 250	°C/W
Power Dissipation@25°C PCB board dimension : 40mm x 40mm (2layer) Copper :1oz		SOT23-5 500	mW
Junction Temperature		150	°C
Storage Temperature		-65 to 150	°C
ESD ⁽⁴⁾	HBM Capability	±2000	V
	CDM Capability	±1500	V
Latch Up Current Maximum Rating ⁽⁴⁾		±200	mA

NOTE:

(1) Stresses beyond those listed under “ABSOLUTE MAXIMUM RATINGS” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(2) Refer to Electrical Characteristics and Application Information for Safe Operating Area.

(3) This particular frame decreases the total thermal resistance of the package and increases its ability to dissipate power when an appropriate area of copper on the printed circuit board is available for heat-sinking.

(4) This device series incorporates ESD protection and is tested by the following methods:

ESD HBM tested per EIA/JESD22-A114;ESD CDM tested per JESD22-C101; Latch up tested per JEDEC78.

ELECTRICAL CHARACTERISTICS

($V_{IN} = V_{OUT} + 2\text{ V}$; $I_{OUT} = 10\text{ mA}$, $C_{IN} = C_{OUT} = 1.0\text{ }\mu\text{F}$, unless otherwise noted. Typical values are at $T_A = +25^\circ\text{C}$.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{IN}^{(1)}$	Operating Input Voltage		3.0		18	V
V_{OUT}	Output Voltage	$T_A = +25^\circ\text{C}$	-2%		+2%	V
		$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	-3%		+3%	
I_{Q_ON}	Quiescent Current	$I_{OUT} = 0\text{ mA}$, $T_A = +25^\circ\text{C}$		1	2	μA
I_{Q_OFF}	Standby Current	$V_{EN} = 0\text{ V}$, $T_A = +25^\circ\text{C}$		0.1	1	μA
LineReg	Line Regulation	$V_{IN} = V_{OUT} + 2\text{ V to } 18\text{ V}$, $I_{OUT} = 10\text{ mA}$ ($\Delta V_{OUT}/\Delta V_{IN}/V_{OUT}$)		0.05	0.20	%/V
$V_{DROP}^{(2)}$	Dropout Voltage	$V_{OUT} = 3.0\text{ V}$, $T_A = +25^\circ\text{C}$		770	1150	mV
		$V_{OUT} = 3.3\text{ V}$, $T_A = +25^\circ\text{C}$		765	1125	
		$V_{OUT} = 3.6\text{ V}$, $T_A = +25^\circ\text{C}$		760	1100	
		$V_{OUT} = 5.0\text{ V}$, $T_A = +25^\circ\text{C}$		750	1075	
LOADReg	Load Regulation	$1\text{ mA} \leq I_{OUT} \leq 500\text{ mA}$, $V_{IN} = V_{OUT} + 2\text{ V}$ $V_{OUT} = 3.3\text{ V}$, $T_A = +25^\circ\text{C}$		30	60	mV
I_{LMT}	Current Limit	$V_{IN} = V_{OUT} + 2\text{ V}$	550	900		mA
V_{ENH}	EN Pin Threshold Voltage	EN Input Voltage "H"	1.2			V
V_{ENL}	EN Pin Threshold Voltage	EN Input Voltage "L"			0.3	V
I_{EN}	EN Pin Current	$V_{EN} = 0 \sim 18\text{ V}$		1		μA
$\text{PSRR}^{(3)}$	Power Supply Rejection Ratio	$f = 1\text{ kHz}$, $V_{IN} = V_{OUT} + 2\text{ V}$ $I_{OUT} = 20\text{ mA}$		60		dB
$e_N^{(3)}$	Output Noise Voltage	$V_{IN} = V_{OUT} + 2\text{ V}$, $I_{OUT} = 1\text{ mA}$, $f = 10\text{ Hz to } 100\text{ KHz}$, $V_{OUT} = 3\text{ V}$, $C_{OUT} = 1\text{ }\mu\text{F}$		120		μVrms
$T_{TSD}^{(3)}$	Thermal Shutdown Temperature	Temperature Increasing from $T_A = +25^\circ\text{C}$		160		$^\circ\text{C}$
$T_{HYS}^{(3)}$	Thermal Shutdown Hysteresis	Temperature Falling from T_{TSD}		20		$^\circ\text{C}$

Note

(1). Here V_{IN} means internal circuit can work normal. If $V_{IN} < V_{OUT}$, Output voltage follow V_{IN} ($I_{OUT} = 1\text{ mA}$), circuit is safety.

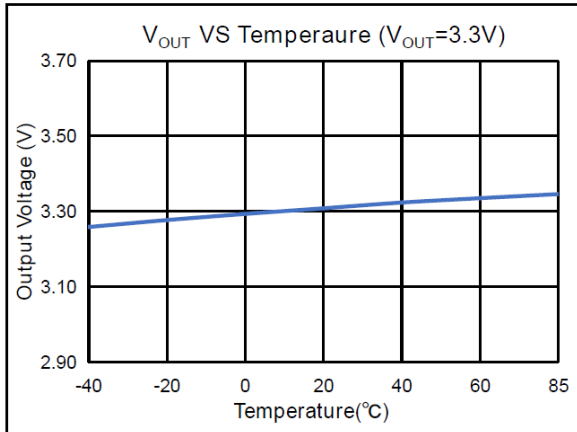
(2). V_{DROP} FT test method: test the V_{OUT} voltage at $V_{SET} + V_{DROPMAX}$ with 500 mA output current.

(3). Guaranteed by design and characterization. not a FT item.

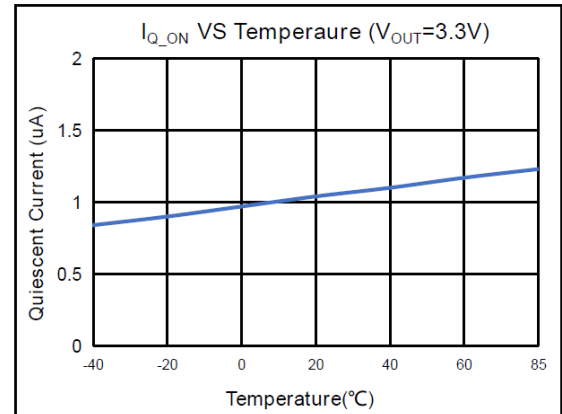
TYPICAL CHARACTERISTICS

VOLTAGE VERSION 3.3 V

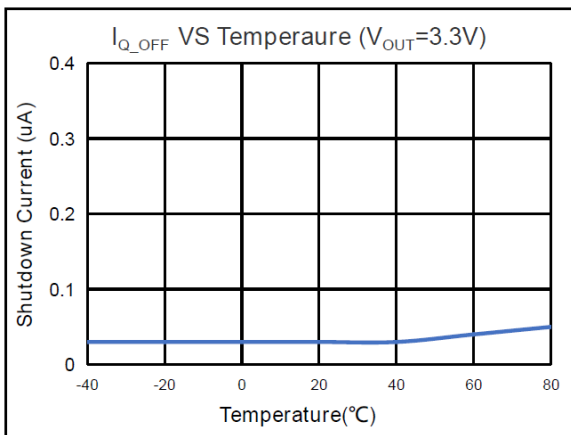
($V_{IN} = V_{OUT} + 2\text{ V}$, $I_{OUT} = 10\text{ mA}$, $C_{IN} = C_{OUT} = 1.0\text{ }\mu\text{F}$, unless otherwise noted. Typical values are at $T_A = +25^\circ\text{C}$.)



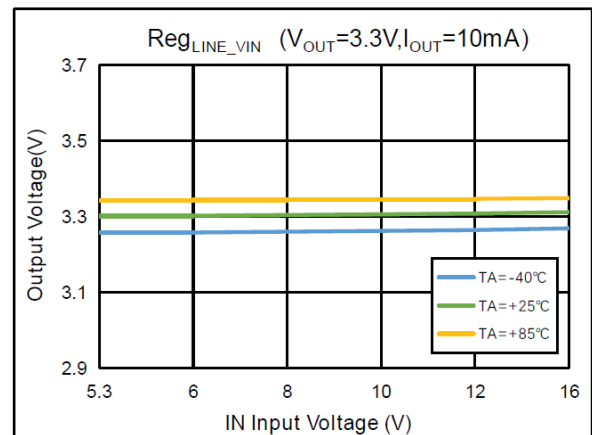
Output Voltage VS Temperature



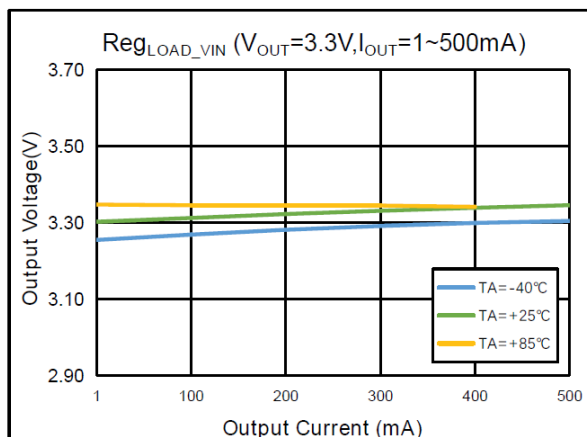
Supply Current VS Temperature



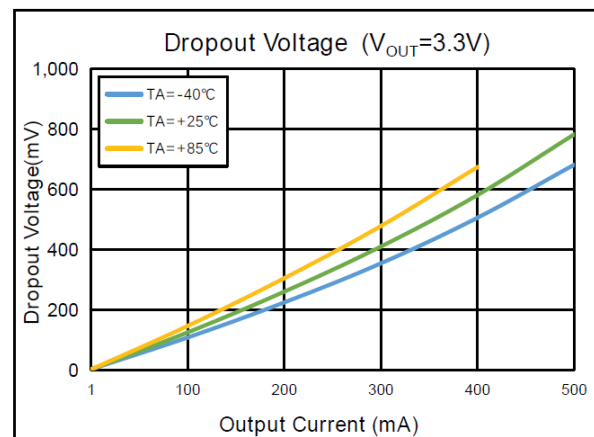
Standby Current VS Temperature



Output Voltage VS Input Voltage ($I_{OUT}=1\text{ mA}$)



Output Voltage VS Output Current

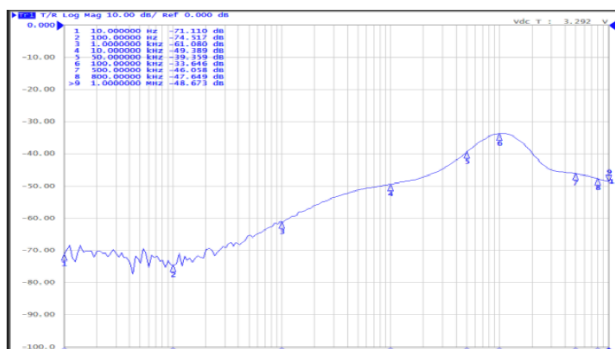


Dropout Voltage VS Output Current

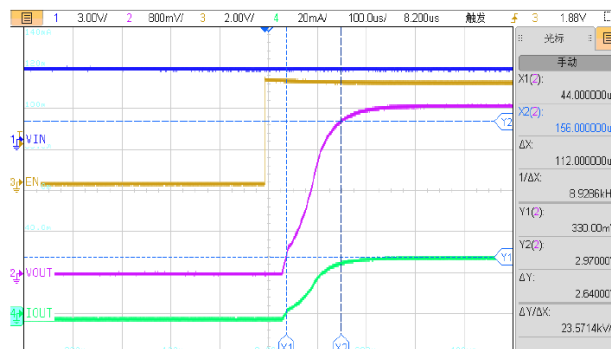
TYPICAL CHARACTERISTICS (Continued)

VOLTAGE VERSION 3.3 V

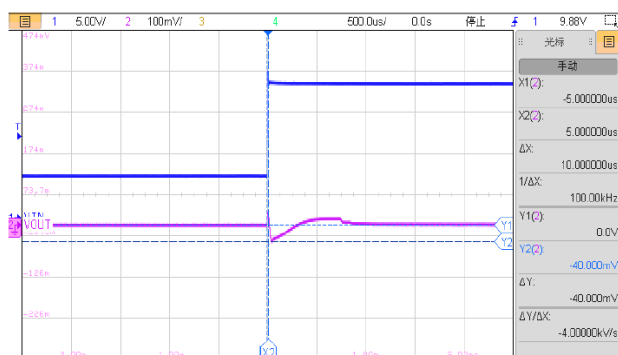
($V_{IN} = V_{OUT} + 2\text{ V}$, $I_{OUT} = 10\text{ mA}$, $C_{IN} = C_{OUT} = 1.0\text{ }\mu\text{F}$, unless otherwise noted. Typical values are at $T_A = +25^\circ\text{C}$.)



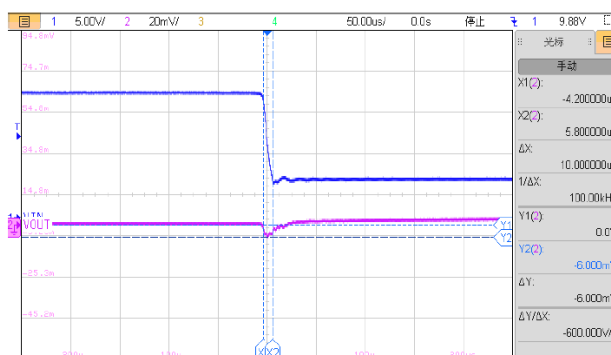
PSRR ($I_{OUT}=20\text{mA}$)



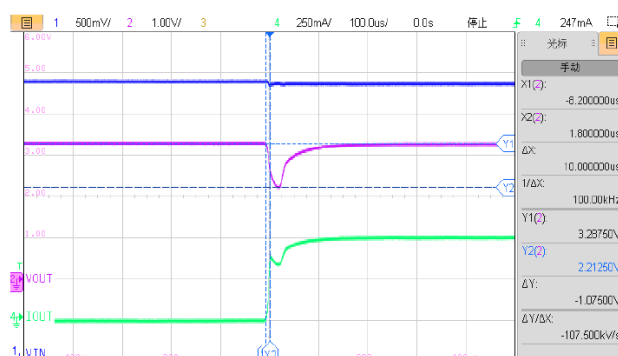
Turn On Speed VS EN Voltage ($I_{OUT}=30\text{mA}$)



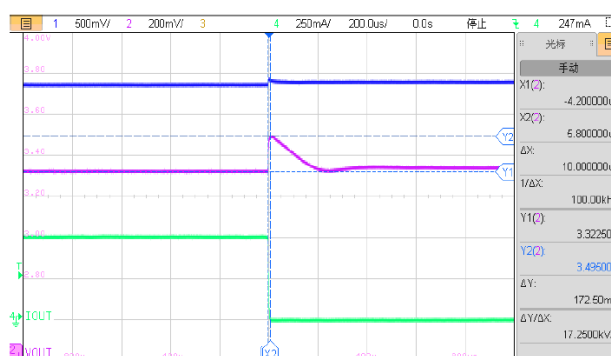
Line Transient Response
 $V_{IN}=5.3\text{V}\sim 16\text{V}$, $V_{OUT}=3.3\text{V}$, $I_{OUT}=1\text{mA}$



Line Transient Response
 $V_{IN}=16\text{V}\sim 5.3\text{V}$, $V_{OUT}=3.3\text{V}$, $I_{OUT}=1\text{mA}$

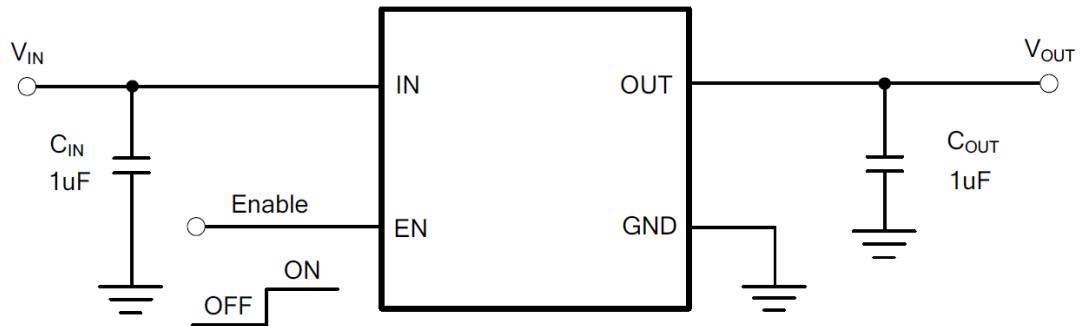


Load Transient Response
 $V_{IN}=5.3\text{V}$, $V_{OUT}=3.3\text{V}$, $I_{OUT}=1\text{mA}\sim 500\text{mA}$



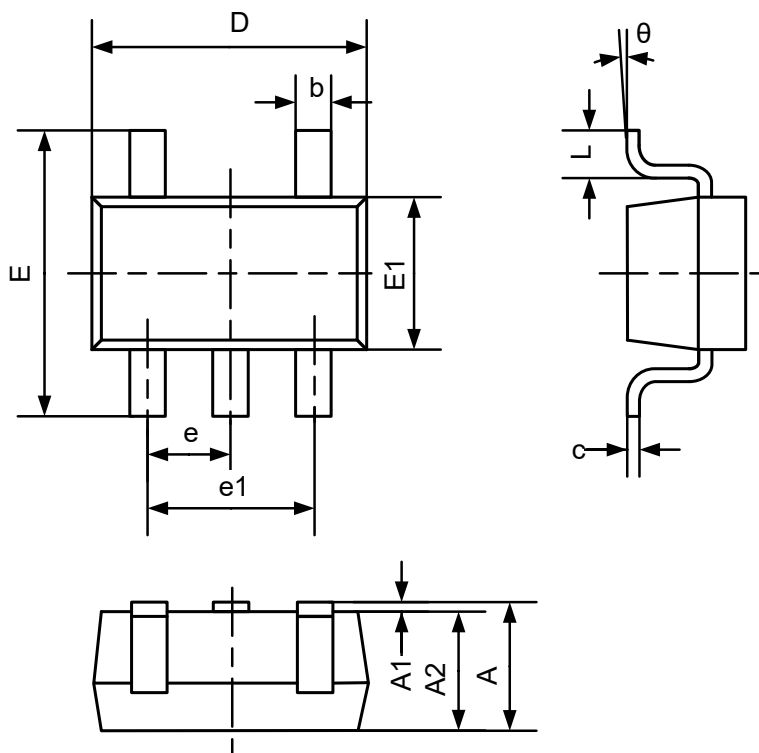
Load Transient Response
 $V_{IN}=5.3\text{V}$, $V_{OUT}=3.3\text{V}$, $I_{OUT}=500\text{mA}\sim 1\text{mA}$

APPLICATION CIRCUITS



PACKAGE DIMENSION

SOT23-5



Symbol	Dimensions In Millimeters	
	MIN	MAX
A	0.700	1.250
A1	0.000	0.100
A2	0.700	1.150
b	0.350	0.500
c	0.080	0.200
D	2.820	3.020
E	2.650	2.950
E1	1.500	1.700
e	0.950BSC	
e1	1.800	2.000
L	0.300	0.600
θ	0°	8°