Dual Channel 8:1 CMOS Analog Signal Multiplexer

DESCRIPTION

The SUM48762 is a CMOS analog IC configured as two groups of 8-channel multiplexers which is completely independent, including power supply. The This CMOS device can operate from 2.5 V to 5.5 V single supplies. Each switch can handle rail-to- rail analog signals. The off-leakage current is only 1 nA (TYP) at +25℃. All digital inputs can support 1.8 V logic control I/O.

The SUM48762 is available in QFN4 x 4-32 package. It operates over an ambient temperature range of -40℃ to +85℃.

FEATURES

- Guaranteed On-Resistance 30 Ω (Ty) with 5 V Supply
- Guaranteed On-Resistance Match Between Channels
- Low Off-Leakage Current 1 nA (TYP) at +25℃
- Low On-Leakage Current 1 nA (TYP) at +25℃
- Optimized Rise Time and Fall Time of A, B, C Control Pins to Reduce Clock Feedthrough Effect
- 2.5 V to 5.5 V Single Supply Operation
- 1.8 V Logic Compatible
- High Off-Isolation: -83 dB (R_L = 50 Ω, f = 1 MHz)
- -40℃to +85℃Operating Temperature Range
- Available in QFN4 × 4-32 Package

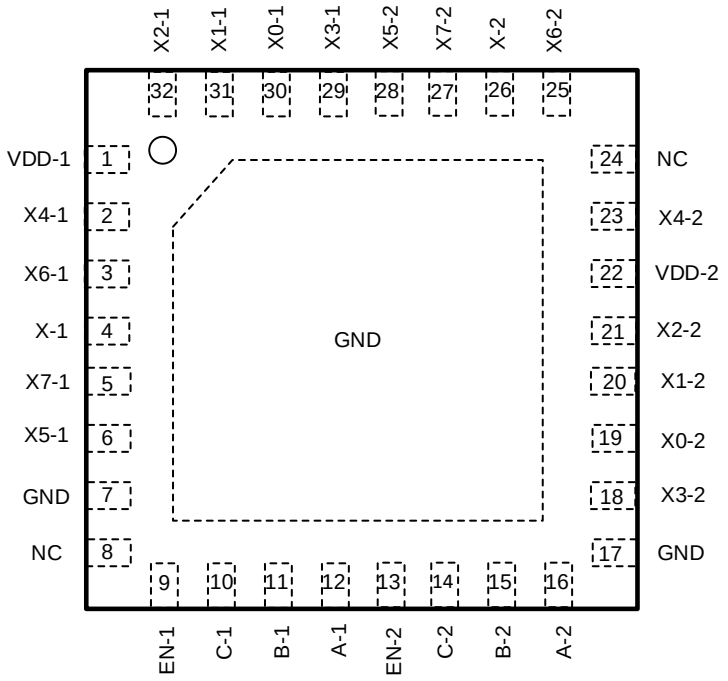
APPLICATIONS

- Battery-Operated Equipment
- Audio and Video Signal Routing
- Low-Voltage Data-Acquisition Systems
- Communications Circuits
- Automotive

ORDER INFORMATION

Model	Package	Ordering Number	Packing Option
SUM48762	QFN4 × 4-32	SUM48762QN32	Tape and Reel, 3000

PIN CONFIGURATION (Top View)



QFN4 × 4-32

Pin QFN4 × 4-32	Symbol	Description
1, 22	VDD	Supply Voltage
2, 3, 5, 6, 18, 19, 20, 21, 23, 25, 27, 28, 29, 30, 31, 32	X0~X7	Analog Switch Inputs X0-X7
4, 26	X	Analog Switch “X” Output.
12, 16	A	Digital Address “A”Input.
11, 15	B	Digital Address “B” Input.
10, 14	C	Digital Address “C” Input.
7, 17	GND	Ground. Connect to digital ground.
8, 24	NC	No Connect.
9,13	$\overline{\text{ENABLE}}$	Digital Enable Input. Normally connected to GND.

FUNCTION TABLE

$\overline{\text{ENABLE}}$ INPUT	SELECT INPUTS			ON SWITCHES
	C	B	A	
H	X	X	X	All Switches Open
L	L	L	L	X-X0
L	L	L	H	X-X1
L	L	H	L	X-X2
L	L	H	H	X-X3
L	H	L	L	X-X4
L	H	L	H	X-X5
L	H	H	L	X-X6
L	H	H	H	X-X7

X = Don't care.

NOTE: Input and output pins are identical and interchangeable. Either may be considered an input or output; signals pass equally well in either direction.

RECOMMENDED OPERATING CONDITIONS

Parameter	Rating	Unit
Supply Voltage Range	2.5 to 5.5	V
Operating Temperature Range	-40 to +85	℃

ABSOLUTE MAXIIMUM RATINGS

Parameter		Rating	Unit
V_{DD} to GND		-0.3 to 6	V
Voltage into Any Terminal(1)		-0.3 to (V_{DD}+ 0.3)	V
Continuous Current into Any Terminal		±20	mA
Peak Current, X_(Pulsed at 1ms, 10% duty cycle)		±40	mA
Junction Temperature		150	°C
Storage temperature		-65 ~ +150	°C
Lead temperature		260 (10 sec.)	°C
ESD	HBM	4000	V

NOTE:

1. Voltages exceeding V_{DD} or GND on any signal terminal are clamped by internal diodes. Limit forward-diode current to maximum current rating.
2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
3. This integrated circuit can be damaged if ESD protections are not considered carefully. SUMSEMI recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

CAUTION

This integrated circuit can be damaged by ESD if you don’t pay attention to ESD protection. SUMSEMI recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

SUMSEMI reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time. Please contact SUMSEMI sales office to get the latestdatasheet.

ELECTRICAL CHARACTERISTICS

V_{DD} = 5.0 V, Full = -40℃ to +85℃, typical values are at T_A = +25℃, unless otherwise noted.

Symbol	Parameter	Conditions	TEMP	Min.	Typ.	Max.	Units
ANALOG SWITCH							
$V_{X\_}$, V_X	Analog Signal Range		Full	GND		V_{DD}	V
R_{ON}	On-Resistance	V_{DD} = 5.0 V, I_X = 1 mA	+25℃		30		Ω
			Full			45	
ΔR_{ON}	On-Resistance Match Between Channels	V_{DD} = 5.0 V, I_X = 1 mA	+25℃		1		Ω
			Full			4	
$R_{FLAT(ON)}$	On-Resistance Flatness	V_{DD} = 5.0 V, I_X = 1 mA	+25℃		9		Ω
			Full			20	
$I_{X\_(OFF)}$	X_Off Leakage Current	V_{DD} = 5.0 V, $V_{X\_}$ = 4.5 V or 0 V V_X = 4.5 V or 0 V	+25℃		1	1000	nA
$I_{X(OFF)}$	X Off Leakage Current	V_{DD} = 5.0 V, $V_{X\_}$ = 4.5 V or 0 V V_X = 4.5 V or 0 V	+25℃		1	1000	nA
$I_{X(ON)}$	X On Leakage Current	V_{DD} = 5.0 V, $V_{X\_}$ = 4.5 V or 0 V	+25℃		1	1000	nA
DIGITAL I/O							
V_{AH},V_{BH},V_{CH} $V_{\overline{ENABLE}}$	Logic Input Logic Threshold High		+25℃	1.7			V
V_{AI},V_{BI},V_{CI} $V_{\overline{ENABLE}}$	Logic Input Logic Threshold Low		+25℃			0.5	V
V_{AH},V_{BH},V_{CH} $V_{\overline{ENABLE}}$	Input-Current High	V_A , V_B , V_C , $V_{\overline{ENABLE}}$ = V_{DD}	+25℃		1	1000	nA
V_{AI},V_{BI},V_{CI}, $V_{\overline{ENABLE}}$	Input-Current Low	V_A , V_B , V_C , $V_{\overline{ENABLE}}$ = 0 V	+25℃		1	1000	nA
DYNAMIC CHARACTERISTICS							
t_{TRANS}	Address Transition Time	$V_{X\_}$ = ± 3 V, R_L = 300 Ω, C_L = 35 pF Test Circuit 1	+25℃		70		ns
t_{ON}	Enable Turn-On Time	$V_{X\_}$ = 3 V, R_L = 300 Ω, C_L = 35 pF Test Circuit 2	+25℃		60		ns
t_{OFF}	Enable Turn-Off Time	$V_{X\_}$ = 3 V, R_L = 300 Ω, C_L = 35 pF Test Circuit 2	+25℃		15		ns
t_R	Internal A, B, C Rise Time		+25℃		45		ns
t_F	Internal A, B, C Fall Time		+25℃		50		ns
t_D	Break-Before-Make Time Delay	$V_{X\_}$ = 3 V, R_L = 300 Ω, C_L = 35 pF, Test Circuit 3	+25℃		45		ns

ELECTRICAL CHARACTERISTICS(CONT.)

V_{DD} = 5.0 V, Full = -40℃ to +85℃, typical values are at T_A = +25℃, unless otherwise noted.

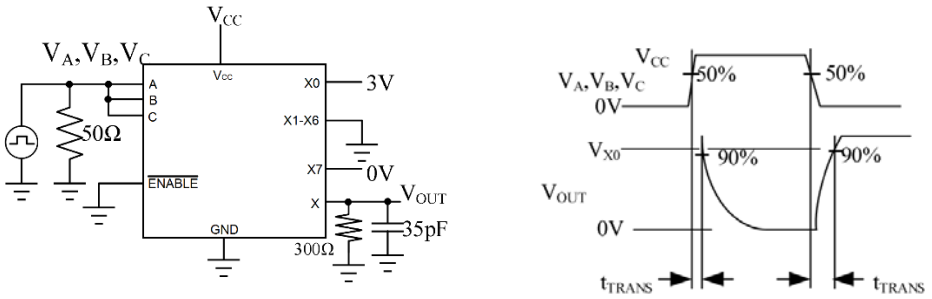
Symbol	Parameter	Conditions	TEMP	Min.	Typ.	Max.	Units
Q	Charge Injection	R_S = 0 Ω, C_L = 1 nF, Test Circuit 4	+25℃		6		PC
O_{ISO}	Off Isolation	R_L = 50 Ω, f = 1 MHz, Test Circuit 5	+25℃		-83		dB
$C_{X\_(OFF)}$	Input Off-Capacitance	$V_{X\_}$ = 0 V, f = 1 MHz, Test Circuit 6	+25℃		4.7		pF
$C_{X(OFF)}$	Output Off-Capacitance	$V_{X\_}$ = 0 V, f = 1 MHz, Test Circuit 6	+25℃		12.7		pF
$C_{X(ON)}$	Output On-Capacitance	$V_{X\_}$ = 0 V, f = 1 MHz, Test Circuit 6	+25℃		16		pF
BW	-3dB Bandwidth	R_L = 50 Ω	+25℃		180		MHz
THD	Total Harmonic Distortion	R_L = 600 Ω, $5V_{P-P}$, f = 20 Hz to 20 kHz	+25℃		0.7		%
POWER SUPPLY							
V_{DD}	Power Supply Range		Full	2.5		5.5	V
I_{DD}	Power Supply Current	V_{DD} = 5.0V, V_A , V_B , V_C , $V_{\overline{ENABLE}}$ = V_{DD} or 0	+25℃		0.1	6	μA

ELECTRICAL CHARACTERISTICS(CONT.)

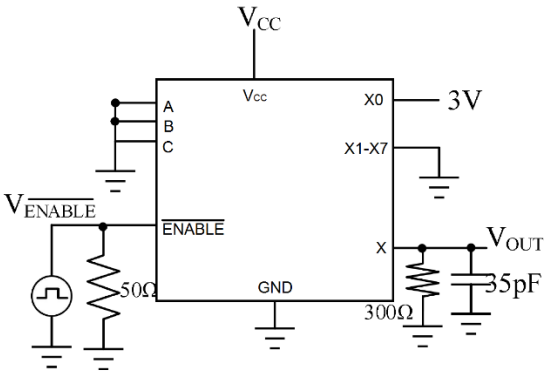
V_{DD} = 3.3 V, Full = -40℃ to +85℃, typical values are at T_A = +25℃, unless otherwise noted.

Symbol	Parameter	Conditions	TEMP	Min.	Typ.	Max.	Units
ANALOG SWITCH							
$V_{X\_}$, V_X	Analog Signal Range		Full	GND		V_{DD}	V
R_{ON}	On-Resistance	I_X = 1 mA	+25℃		65		Ω
			Full			80	
$I_{X\_(OFF)}$	X_Off Leakage Current	$V_{X\_}$ = 1 V, 3 V, V_X = 3 V, 1 V	+25℃		1	1000	nA
$I_{X(OFF)}$	X Off Leakage Current	$V_{X\_}$ = 1 V, 3 V, V_X = 3 V, 1 V	+25℃		1	1000	nA
$I_{X(ON)}$	X On Leakage Current	V_X = 3 V, 1 V	+25℃		1	1000	nA
DIGITAL I/O							
V_{AH},V_{BH},V_{CH}, $V_{\overline{ENABLE}}$	Logic Input Logic Threshold High		+25℃	1.7			V
V_{AI},V_{BI},V_{CI}, $V_{\overline{ENABLE}}$	Logic Input Logic Threshold Low		+25℃			0.5	V
I_{AH},, I_{BH}, I_{CH}, $V_{\overline{ENABLE}}$	Input-Current High	V_A , V_B , V_C $V_{\overline{ENABLE}}$ = V_{DD}	+25℃		1	1000	nA
I_{AI},I_{BI},I_{CI}, $V_{\overline{ENABLE}}$	Input-Current Low	V_A , V_B , V_C $V_{\overline{ENABLE}}$ = 0 V	+25℃		1	1000	nA
DYNAMIC CHARACTERISTICS							
t_{TRANS}	Address Transition Time	$V_{X\_}$ = 3 V/0 V, R_L = 300 Ω C_L = 35 pF, Test Circuit 1	+25℃		100		ns
t_{ON}	Enable Turn-On Time	$V_{X\_}$ = 3 V, R_L = 300 Ω C_L = 35 pF, Test Circuit 2	+25℃		80		ns
t_{OFF}	Enable Turn-Off Time	$V_{X\_}$ = 3 V, R_L = 300 Ω C_L = 35 pF, Test Circuit 2	+25℃		15		ns
t_R	Internal A, B, C Rise Time		+25℃		80		ns
t_F	Internal A, B, C Fall Time		+25℃		85		ns
t_D	Break-Before-Make Time Delay	$V_{X\_}$ = 3 V, R_L = 300 Ω C_L = 35 pF, Test Circuit 3	+25℃		65		ns
BW	-3dB Bandwidth	R_L = 50 Ω	+25℃		180		MHz
Q	Charge Injection	R_S = 0 Ω, C_L = 1 nF, V_S = 2.5 V, Test Circuit 4	+25℃		4		PC
POWER SUPPLY							
I_{DD}	Power Supply Current	V_A , V_B , V_C $V_{\overline{ENABLE}}$ = V_{DD} or 0	+25℃		0.1	3	μA

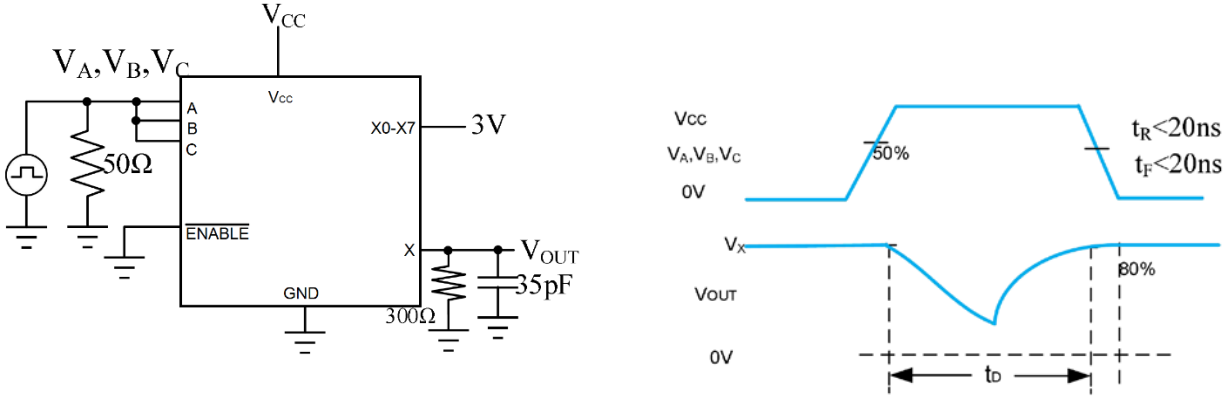
TEST CIRCUITS



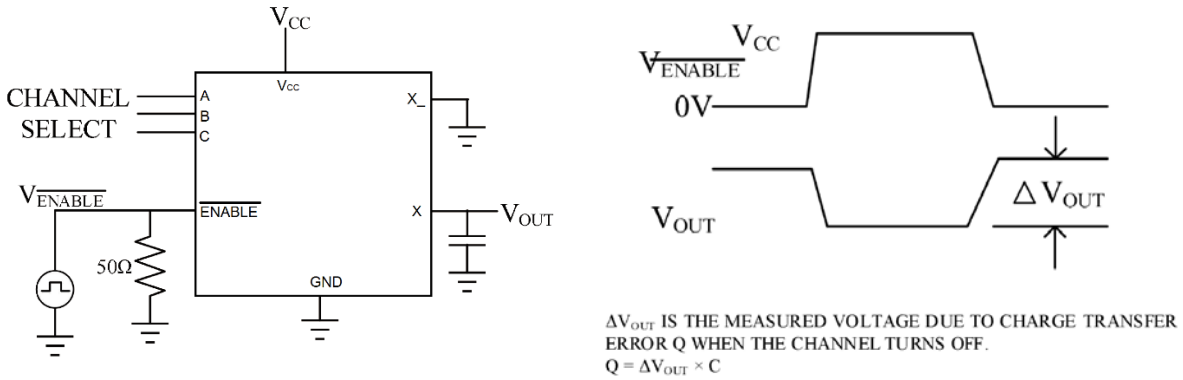
Test Circuit 1 Address Transition Times (t_{TRANS})



Test Circuit 2 Switching Times (t_{ON}, t_{OFF})

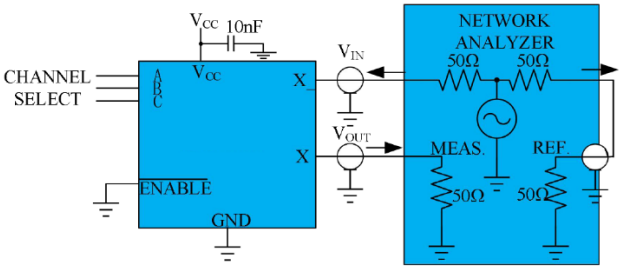


Test Circuit 3 Break-Before-Make Time (t_D)



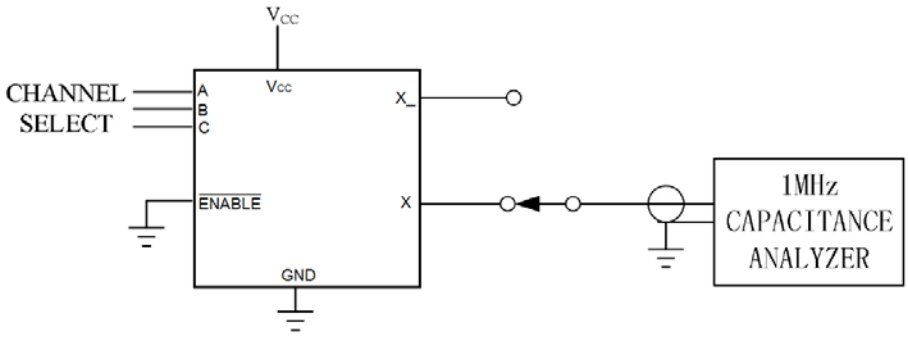
ΔV_{OUT} IS THE MEASURED VOLTAGE DUE TO CHARGE TRANSFER ERROR Q WHEN THE CHANNEL TURNS OFF.
$Q = \Delta V_{OUT} \times C$

Test Circuit 4 Charge Injection (Q)



MEASUREMENTS ARE STANDARDIZED AGAINST SHORT AT SOCKET TERMINALS.
OFF-ISOLATION IS MEASURED BETWEEN COM AND "OFF" NO TERMINAL ON EACH SWITCH.
ON-LOSS IS MEASURED BETWEEN COM AND "ON" NO TERMINAL ON EACH SWITCH.
SIGNAL DIRECTION THROUGH SWITCH IS REVERSED; WORSE VALUES ARE RECORDED.

Test Circuit 5 Off Isolation, On Loss



Test Circuit 6 Capacitance

APPLICATION INFORMATION

Power-Supply Considerations Overview

The SUM48762 construction is typical of most CMOS analog switch. It supports single power supply. V_{DD} and GND are used to drive the internal CMOS switches and set the limits of the analog voltage on any switch. Reverse ESD protection diodes are internally connected between each analog-signal pin and both V_{DD} and GND. If any analog signal exceeds V_{DD} or GND, one of these diodes will conduct. During normal operation, these and other reverse-biased ESD diodes leak, forming the only current drawn from V_{DD} or GND.

Virtually all the analog leakage current comes from the ESD diodes. Although the ESD diodes on a given signal pin are identical and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V_{DD} or GND and the analog signal. This means their leakages will vary as the signal varies. The difference in the two diode leakages to the V_{DD} and GND pins constitutes the analog-signal-path leakage current. All analog leakage current flows between each pin and one of the supply terminals, not to the other switch terminal. This is why both sides of a given switch can show leakage currents of either the same or opposite polarity.

Over-Voltage Protection

Proper power-supply sequencing is recommended for the CMOS device. Do not exceed the absolute maximum ratings because stresses beyond the listed ratings can cause permanent damage to the devices. Always sequence V_{DD} on first, followed by the logic inputs and analog signals. If power-supply sequencing is not possible, add one 100 Ω resistor in series with the supply V_{DD} pin for over-voltage protection (Figure 1).

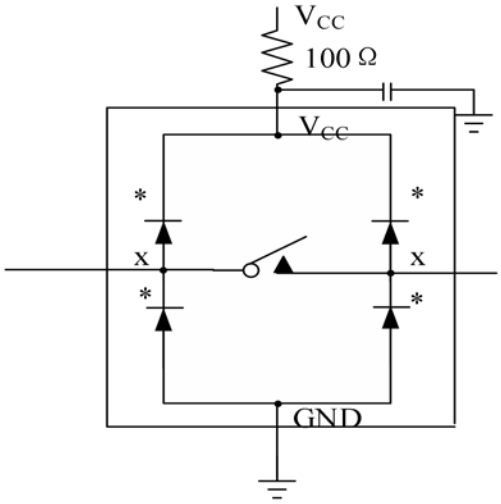
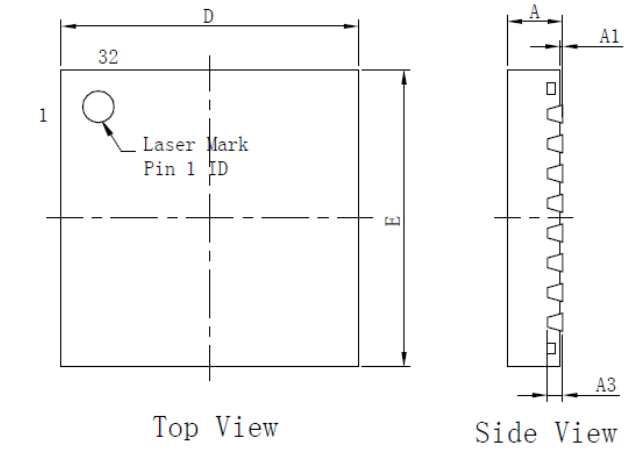
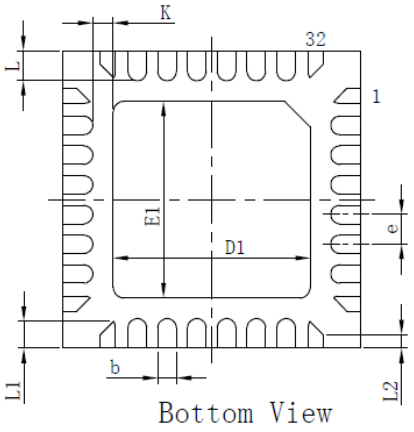


Figure 1 Over-Voltage Protection Using External Resistor

PACKAGE OUTLINE

QFN4 × 4-32





Symbol	Dimensions In Millimeters		
	Min	Typ.	Max
A	0.700	0.750	0.800
A1	0.000	—	0.050
A3	0.203REF		
b	0.150	0.200	0.250
D	3.900	4.000	4.100
E	3.900	4.000	4.100
D1	2.550	2.65	2.75
E1	2.550	2.65	2.75
e	0.400TYP		
K	0.200	—	—
L	0.300	0.400	0.500
L1	0.310	0.360	0.410
L2	0.130	0.180	0.230

V 1.0