4-Bit 100 Mb/s Configurable Dual-Supply Level Translator

DESCRIPTION

The SUM5014 is a 4-bit bidirectional level translator in which the input and output ports are switched automatically without direction control. The data path of each channel can be either from I/O_V_{Ln} to I/O_V_{CCn} or from I/O_V_{CCn} to I/O_V_{Ln}. All of the I/O ports are designed to track two different power supply rails, V_{CC} and V_L respectively. Both of the supply voltage are configurable from 1.2 V to 4.5 V. The V_{CC} and V_L supplies are independent which allows a logic signal on the V_L side to be translated to either a higher or a lower logic signal voltage on the V_{CC} side, and vice-versa.

The SUM5014 has high output current capability, which allows the translator to drive high capacitive loads such as most high frequency EMI filters. The enable pin(EN) is used to reduce the power consumption. The EN pin can be used to disable both I/O ports by putting them in 3-state which significantly reduces the supply current from both V_{CC} and V_L. The EN signal is referenced to the V_L supply.

FEATURES

- Wide V_{CC}, V_L Operating Range: 1.2 V to 4.5 V
- V_L and V_{CC} are independent
  V_L may be greater than, equal to, or less than V_{CC}
- High 100 pF Capacitive Drive Capability
- High−Speed with 120 Mb/s Guaranteed Date Rate for V_{CC}, V_L > 2.3 V
- Low Bit−to−Bit Skew
- Overvoltage Tolerant Enable and I/O Pins
- Non−preferential Power up Sequencing
- Power−Off Protection
- Small packaging: UQFN1.7 × 2.0-12
- These are Pb−Free Devices
- ESD ≥ 8000 V (HBM) ; Latch-up ≥ 500 mA

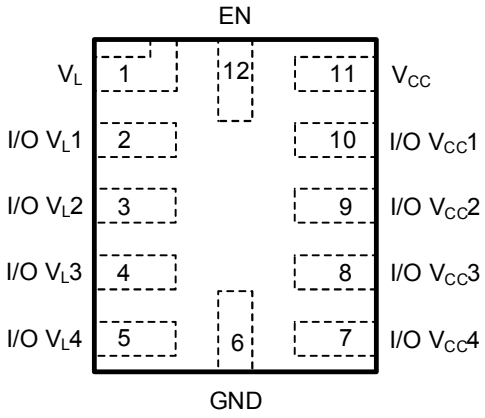
APPLICATION

- Mobile Phones, PDAs, Other Portable Devices

ORDER INFORMATION

Model	Package	Ordering Number	Packing Option
SUM5014	UQFN1.7 × 2.0-12	SUM5014UQN12	Tape and Reel

PIN CONFIGURATION (Top View)

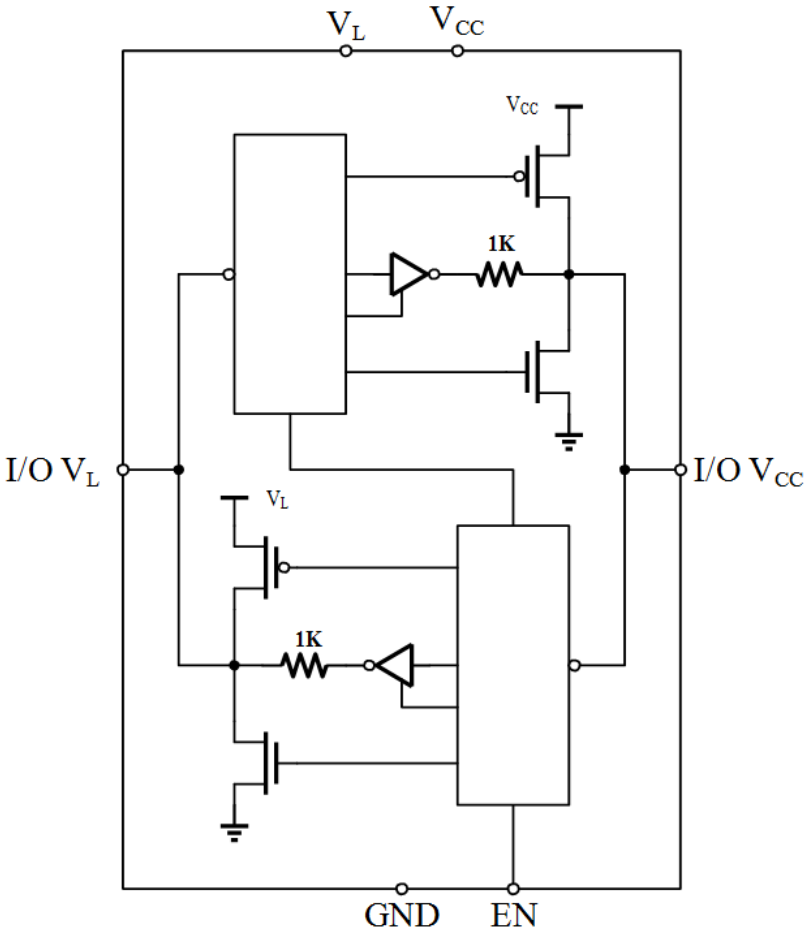


UQFN1.7 × 2.0-12

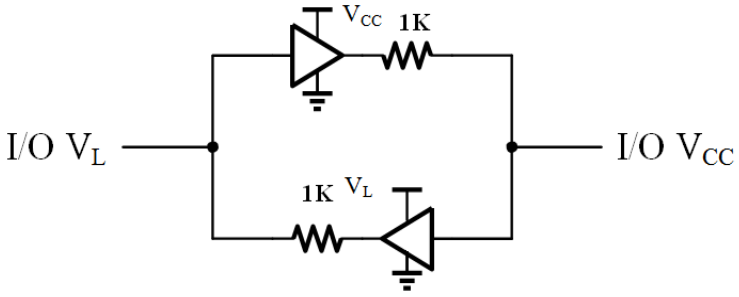
PIN DESCRIPTIONS

Pin Name	Description
V_{CC}	V_{CC} Input Voltage
V_L	V_L Input Voltage
GND	Ground
EN	Output Enable
I/O V_{CCn}	I/O Port, Referenced to V_{CC}
I/O V_{Ln}	I/O Port, Referenced to V_L

BLOCK DIAGRAM



Simplified Functional Diagram (1 channel)



Logic Diagram (1 channel)

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Condition	Unit
V_{CC}	High−side DC Supply Voltage	−0.5 to +5.5		V
V_L	Low−side DC Supply Voltage	−0.5 to +5.5		V
I/O V_{CC}	V_{CC}−Referenced DC Input/Output Voltage	−0.5 to +5.5		V
I/O V_L	V_L−Referenced DC Input/Output Voltage	−0.5 to +5.5		V
V_I	Enable Control Pin DC Input Voltage	−0.5 to +5.5		V
I_{IK}	DC Input Diode Current	-50	V_I < GND	mA
I_{OK}	DC Output Diode Current	-50	V_O < GND	mA
I_{CC}	DC Supply Current Through V_{CC}	±100		mA
I_L	DC Supply Current Through V_L	±100		mA
I_{GND}	DC Ground Current Through Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		℃

NOTE:

Stresses beyond those listed under “ABSOLUTE MAXIMUM RATINGS” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

This integrated circuit can be damaged by ESD if you don’t pay attention to ESD protection. SUMSEMI recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

SUMSEMI reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time. Please contact SUMSEMI sales office to get the latest datasheet.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	High−side Positive DC Supply Voltage		1.2	4.5	V
V_L	Low−side Positive DC Supply Voltage		1.2	4.5	V
V_I	Enable Control Pin Voltage		GND	4.5	V
V_{IO}	Bus Input/Output Voltage	I/O V_{CC}	GND	4.5	V
		I/O V_L	GND	4.5	
T_A	Operating Temperature Range		-55	+125	℃
Δt/ΔV	Input Transition Rise or Rate V_I, V_{IO} from 30% to 70% of V_{CC}; V_{CC} = 3.3 V ± 0.3 V		0	10	ns

ELECTRICAL CHARACTERISTICS

(Note: V_S is the corresponding supply for IO, i.e. V_{CC} for IO_V_{CC} and V_L for IO_V_L)

Symbol	Parameter	Test Conditions (1)	V_{CC} (2)	V_L (3)	−40℃ to +85℃			−55℃ to +125℃		Unit
					Min	Typ (4)	Max	Min	Max	
V_{IH}	I/O Input HIGH Voltage		1.2~4.5	1.2~4.5	2/3*V_S			2/3*V_S		V
V_{IL}	I/O Input LOW Voltage		1.2~4.5	1.2~4.5			1/3*V_S		1/3*V_S	V
V_{IH-EN}	Control Pin Input HIGH Voltage	T_A = +25℃	1.2~4.5	1.2~4.5	2/3*V_L			2/3*V_L		V
V_{IL-EN}	Control Pin Input LOW Voltage	T_A = +25℃	1.2~4.5	1.2~4.5			1/3*V_L		1/3*V_L	V
V_{OH}	I/O Output HIGH Voltage	I/O source current = 20 μA	1.2~4.5	1.2~4.5	0.9*V_S			0.9*V_S		V
V_{OL}	I/O Output LOW Voltage	I/O sink Current = 20 μA	1.2~4.5	1.2~4.5			0.2		0.2	V
I_Q	Static Supply Current	EN = V_L, I_O = 0 A, (I/O -in = 0 V or V_S, I/O-out = float)	1.2~4.5	1.2~4.5			1		2.5	μA
I_{TS}	Tristate Output Mode Supply Current	T_A = 25℃, EN = 0 V, (I/O-in = 0 V or V_S, I/O-out = float)	1.2~4.5	1.2~4.5			0.5		1.5	μA
I_{OZ}	I/O Tristate Output Mode Leakage Current	T_A = +25℃, EN = 0 V	1.2~4.5	1.2~4.5			±1		±1.5	μA
I_I	Control Pin Input Current	T_A = +25℃	1.2~4.5	1.2~4.5			±1		±1	μA
I_{OFF}	Power off Leakage Current	I/O V_{CC} = 0 to 4.5 V, I/O V_L = 0 to 4.5 V	0	0			1		1.5	μA
			1.2~4.5	0			1		1.5	
			0	1.2~4.5			1		1.5	

Notes:

1. Normal test conditions are V_I = 0 V, C_{IOVCC} ≤ 15 pF and C_{IOVL} ≤ 15 pF, unless otherwise specified.
2. V_{CC} is the supply voltage associated with the I/O V_{CC} port, and V_{CC} ranges from +1.2 V to 4.5 V under normal operating conditions.
3. V_L is the supply voltage associated with the I/O V_L port, and V_L ranges from +1.2 V to 4.5 V under normal operating conditions.
4. Typical values are for V_{CC} = +2.8 V, V_L = +1.8 V and T_A = +25℃. All units are production tested at T_A = 25℃. Limits over the operating temperature range are guaranteed by design.

TIMING CHARACTERISTICS

Symbol	Parameter		Test Conditions[5]	V_{CC}[6]	V_L[7]	−55℃ to +125℃			Unit
						Min	Typ[8]	Max	
T_R	I/O Rise Time		C_{IO} = 15 pF	1.2 ~ 4.5	1.2 ~ 4.5			9.5	ns
				1.8 ~ 4.5	1.8 ~ 4.5			7.5	
T_F	I/O Fall Time		C_{IO} = 15 pF	1.2 ~ 4.5	1.2 ~ 4.5			9.5	ns
				1.8 ~ 4.5	1.8 ~ 4.5			7.5	
Z_{OVCC}	I/O V_{CC} One−Shot Output Impedance		[9]	1.8 4.5	1.2 ~ 4.5		20 6.0		Ω
Z_{OVL}	I/O V_L One−Shot Output Impedance		[9]	1.2 ~ 4.5	1.8 4.5		20 6.0		Ω
t_{PD}	Propagation Delay (Driving I/O V_{CC} or I/O V_L)		C_{IOVCC} = 15 pF	1.2 ~ 4.5	1.2 ~ 4.5			35	ns
				1.8 ~ 4.5	1.8 ~ 4.5			10	
			C_{IOVCC} = 30 pF	1.2 ~ 4.5	1.2 ~ 4.5			35	
				1.8 ~ 4.5	1.8 ~ 4.5			15	
			C_{IOVCC} = 50 pF	1.2 ~ 4.5	1.2 ~ 4.5			37	
				1.8 ~ 4.5	1.8 ~ 4.5			15	
			C_{IOVCC} = 100 pF	1.2 ~ 4.5	1.2 ~ 4.5			40	
				1.8 ~ 4.5	1.8 ~ 4.5			16	
t_{SK}	Channel−to−Channel Skew		C_{IOVCC} = C_{IOVL} = 15 pF [9]	1.2 ~ 4.5	1.2 ~ 4.5			0.15	ns
I_{IN_PEAK}	Input Driver Maximum Peak Current		EN = V_L; I/O_V_{CC} = 1 MHz Square Wave, Amplitude = V_{CC}, or I/O_V_L = 1 MHz Square Wave, Amplitude = V_L [9]	1.2 ~ 4.5	1.2 ~ 4.5			5.0	mA
t_{EN}	I/O Output Enable Time	t_{PZH}	C_{IO} = 15 pF, I/O_V_L = V_L	1.2 ~ 4.5	1.2 ~ 4.5			160	ns
		t_{PZL}	C_{IO} = 15 pF, I/O_V_L = 0 V	1.2 ~ 4.5	1.2 ~ 4.5			130	
t_{DIS}	I/O Output Disable Time	t_{PHZ}	C_{IO} = 15 pF, I/O_V_L= V_L	1.2 ~ 4.5	1.2 ~ 4.5			210	ns
		t_{PLZ}	C_{IO} = 15 pF, I/O_V_L = 0 V	1.2 ~ 4.5	1.2 ~ 4.5			175	
MDR	Maximum Data Rate		C_{IO} = 15 pF	1.5 ~ 4.5	1.5 ~ 4.5			60	Mbps
				2.3 ~ 4.5	2.3 ~ 4.5			140	
			C_{IO} = 30 pF	1.6 ~ 4.5	1.5 ~ 4.5			60	
				2.3 ~ 4.5	2.3 ~ 4.5			120	
			C_{IO} = 50 pF	1.5 ~ 4.5	1.5 ~ 4.5			60	
				2.3 ~ 4.5	2.3 ~ 4.5			100	
			C_{IO} = 100 pF	1.5 ~ 4.5	1.5 ~ 4.5			40	
				2.3 ~ 4.5	2.3 ~ 4.5			60	

Notes:

5. Normal test conditions are V_I = 0 V, C_{IOVCC} ≤ 15 pF and C_{IOVL} ≤ 15 pF, unless otherwise specified.
6. V_{CC} is the supply voltage associated with the I/O V_{CC} port, and V_{CC} ranges from +1.2 V to 4.5 V under normal operating conditions.
7. V_L is the supply voltage associated with the I/O V_L port, and V_L ranges from +1.2 V to 4.5 V under normal operating conditions.
8. Typical values are for V_{CC} = +2.8 V, V_L = +1.8 V and T_A = +25℃. All units are production tested at T_A = +25℃. Limits over the operating temperature range are guaranteed by design.
9. Guaranteed by design.
10. Normal test conditions are V_I = 0 V, C_{IOVCC} ≤ 1 pF and C_{IOVL} ≤ 15 pF, unless otherwise specified.
11. V_{CC} is the supply voltage associated with the I/O V_{CC} port, and V_{CC} ranges from +1.2 V to 4.5 V under normal operating conditions.
12. V_L is the supply voltage associated with the I/O V_L port, and V_L ranges from +1.2 V to 4.5 V under normal operating conditions.
13. Typical values are for V_{CC} = +2.8 V, V_L = +1.8 V and T_A = +25℃. All units are production tested at T_A = +25℃. Limits over the operating temperature range are guaranteed by design.

FUNCTION DESCRIPTION

The SUM5014 auto−sense translator provides bi−directional logic voltage level shifting to transfer data in multiple supply voltage systems. These level translators have two supply voltages, V_L and V_{CC}, which set the logic levels on the input and output sides of the translator. When used to transfer data from the I/O V_L to the I/O V_{CC} ports, input signals referenced to the V_L supply are translated to output signals with a logic level matched to V_{CC}. In a similar manner, the I/O V_{CC} to I/O V_L translation shifts input signals with a logic level compatible to V_{CC} to an output signal matched to V_L.

The SUM5014 translator consists of bi−directional channels that independently determine the direction of the data flow without requiring a directional pin. One−shot circuits are used to detect the rising or falling input signals. In addition, the one−shots decrease the rise and fall times of the output signal for high−to−low and low −to−high transitions.

Auto−sense translators such as the SUM5014 have a wide bandwidth, but a relatively small DC output current rating. The high bandwidth of the bi−directional I/O circuit is used to quickly transform from an input to an output driver and vice versa. The I/O ports have a modest DC current output specification so that the output driver can be over driven when data is sent in the opposite direction. For proper operation, the input driver to the auto−sense translator should be capable of driving 2 mA of peak output current. The bi−directional configuration of the translator results in both input stages being active for a very short time period. Although the peak current from the input signal circuit is relatively large, the average current is small and consistent with a standard CMOS input stage.

The SUM5014 translator has an Enable pin (EN) that provides tri−state operation at the I/O pins. Driving the Enable pin to a low logic level minimizes the power consumption of the device and drives the I/O V_{CC} and I/O V_L pins to a high impedance state. Normal translation operation occurs when the EN pin is equal to a logic high signal. The EN pin is referenced to the V_L supply and has Over−Voltage Tolerant (OVT) protection.

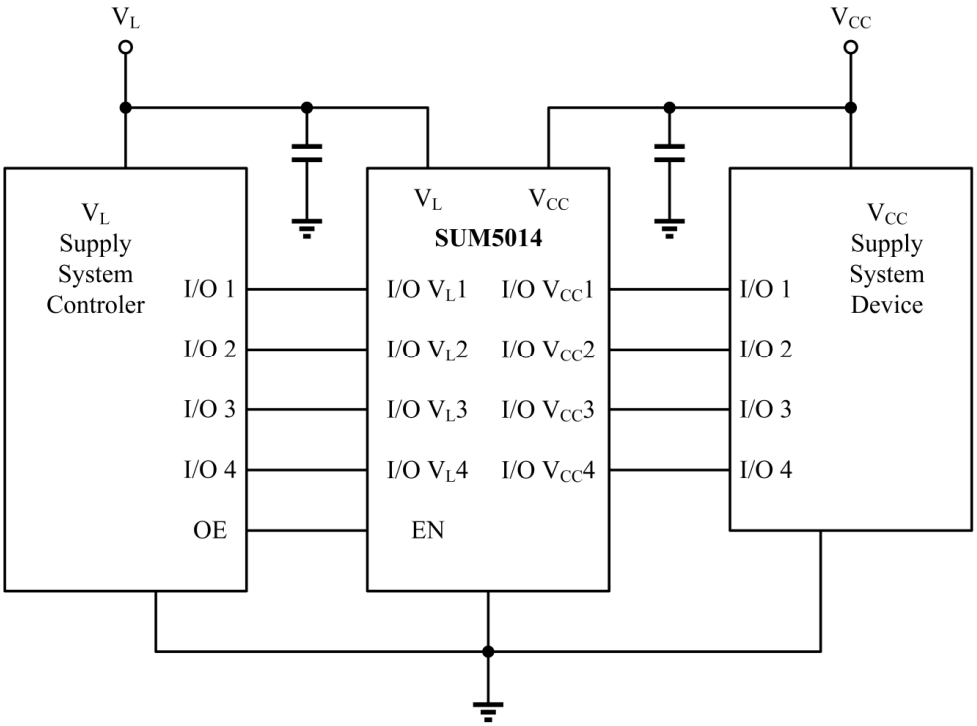
The SUM5014 translator can function as a non−inverting uni−directional translator. One advantage of using the translator as a uni−directional device is that each I/O pin can be configured as either an input or output. The configurable input or output feature is especially useful in applications such as SPI that use multiple uni−directional I/O lines to send data to and from a device. The flexible I/O port of the auto sense translator simplifies the trace connections on the PCB.

The values of the V_L and V_{CC} supplies can be set to anywhere between 1.2 V and 4.5 V. Design flexibility is maximized because V_L may be either greater than or less than the V_{CC} supply. In contrast, the majority of the competitive auto sense translators has a restriction that the value of the V_L supply must be equal to less than (V_{CC}−0.4) V.

The sequencing of the power supplies will not damage the device during power−up operation. In addition, the I/O V_{CC} and I/O V_L pins are in the high impedance state if either supply voltage is equal to 0 V. For optimal performance, 0.01 μF to 0.1 μF decoupling capacitors should be used on the V_L and V_{CC} power supply pins. Ceramic capacitors are a good design choice to filter and bypass any noise signals on the voltage lines to the ground plane of the PCB. The noise immunity will be maximized by placing the capacitors as close as possible to the supply and ground pins, along with minimizing the PCB connection traces.

The SUM5014 translators have a power down feature that provides design flexibility. The output ports are disabled when either power supply is off (V_L or V_{CC} = 0 V). This feature causes all of the I/O pins to be in the power saving high impedance state.

APPLICATION CIRCUITS

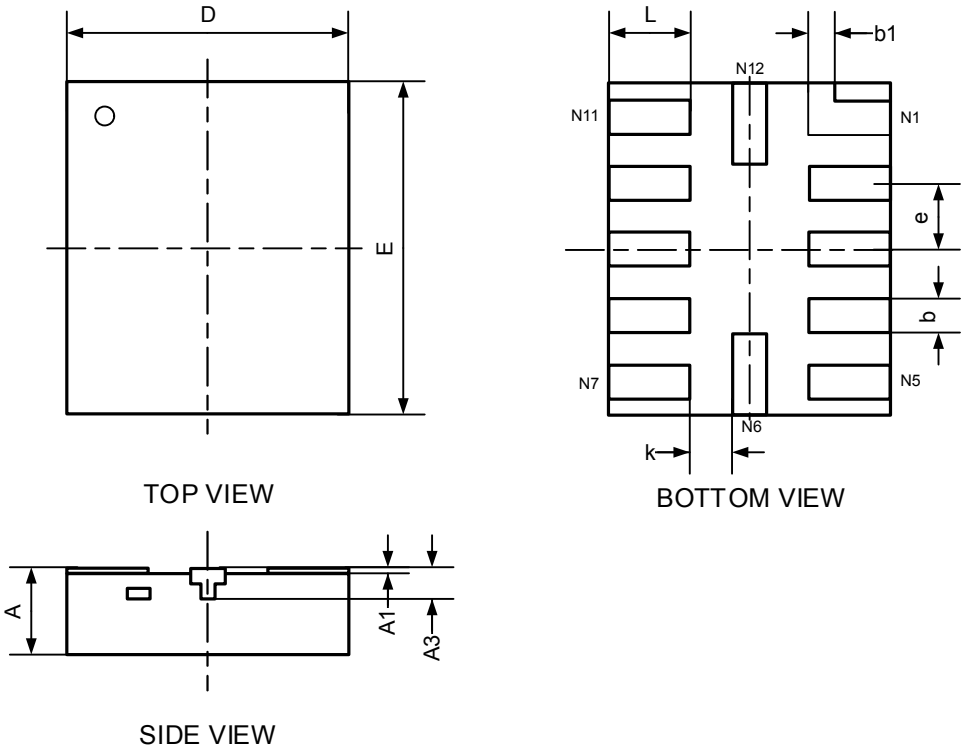


Typical Application Circuit

* : This electric circuit only supplies for reference.

PACKAGE OUTLINE

UQFN1.7 × 2.0-12



Symbol	Dimensions in Millimeters	
	Min	Max
A	0.450	0.550
A1	0.000	0.050
A3	0.152REF	
D	1.600	1.800
E	1.900	2.100
b	0.150	0.250
b1	0.150REF	
k	0.250REF	
e	0.400BSC	
L	0.400	0.600