

High efficiency, 2 A synchronous rectification Step-Down Converter

FEATURES

- 2.5 V ~ 6 V input voltage range
- 35 μ A ultra-low quiescent current
- Internal soft-start reduces chip stress
- Short circuit protection Hiccup mode
- Internal integrated low $R_{DS(ON)}$ switch
- Over Voltage Protection
- 1.5MHz switching frequency minimizes external components
- Optimized PFM mode for battery applications to improve light-load efficiency and extend battery life
- 100% duty cycle supports input and output low dropout operation
- Available in SOT23-5, SOT23-6

DESCRIPTION

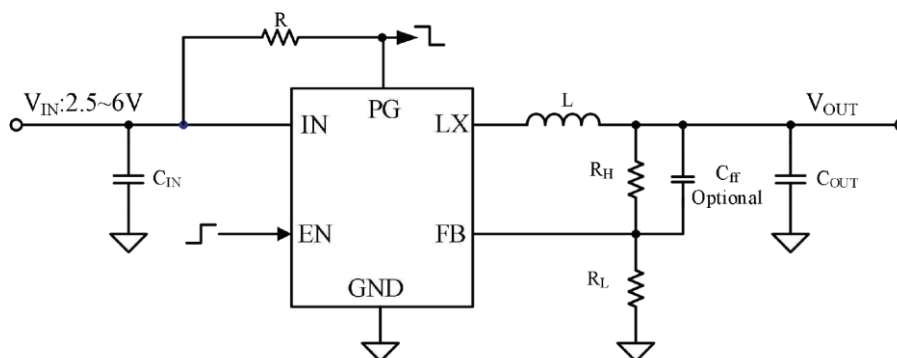
The SUM5202 is a high-efficiency synchronous Buck converter that can operate over a wide input voltage range of 2.5 V to 6 V and can deliver up to 2 A of output current. It integrates the main switch and synchronous switch inside, and has extremely low on-resistance to reduce conduction loss. The switching frequency is 1.5 MHz, which can reduce the size of the external inductor and output capacitor and reduce the output voltage ripple.

The SUM5202 is available in SOT23-5 and SOT23-6 packages.

APPLICATIONS

- Set-top box, security camera
- Mobile phones, handheld game consoles, media players
- Electric toys, meters, etc.

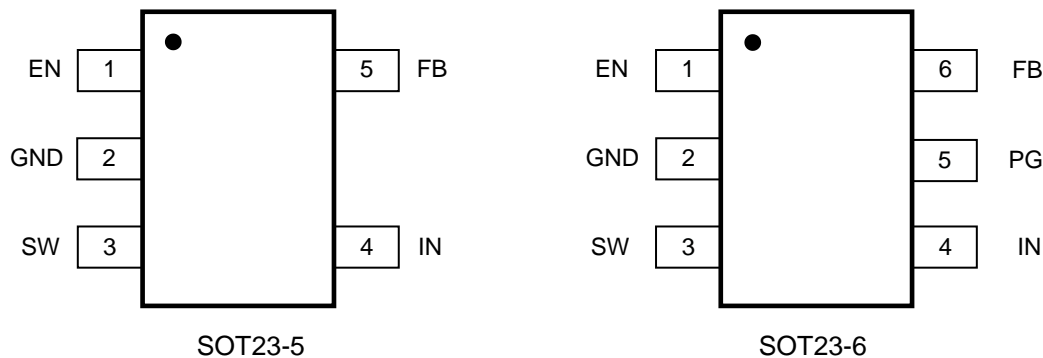
APPLICATION CIRCUITS



ORDERING INFORMATION

Model	Package	Ordering Number	Packing Option
SUM5202	SOT23-5	SUM5202KA5	Tape and Reel, 3000
	SOT23-6	SUM5202KA6	Tape and Reel, 3000

PIN CONFIGURATION (Top View)



PIN DESCRIPTIONS

Pin		Name	Function
SOT23-5	SOT23-6		
1	1	EN	Enable signal input pin, the chip works when input high level, do not leave the pin floating.
2	2	GND	Ground Pin.
3	3	SW	Inductor pin. This pin should be connected to the switching node of the inductor.
4	4	IN	Power input pin. Use a ceramic decoupling capacitor of at least 4.7uF to connect this pin to ground.
-	5	PG	Power good pin, indicating whether the output power is ready.
5	6	FB	Feedback pin. Connect this pin to the center point of the output divider resistor to set the output voltage.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Parameter		Value	Unit
IN Pin Voltage Range to GND		-0.3 to 6.5	V
SW Pin Voltage Range to GND		-0.3 to 6.5	V
EN, FB, PG Voltage		-0.3 to 6.5	V
Ambient Temperature (T _A)		-40 to 85	°C
Storage Temperature Range (T _{STG})		-55 to 150	°C
Thermal Resistance, Junction to Ambient (θ_{JA}) ⁽²⁾	SOT23-5	250	°C/W
	SOT23-6	220	
Thermal Resistance, Junction to Case (θ_{JC})		130	°C/W
ESD	HBM	2000	V
	CDM	1000	

NOTE:

- 1) Stresses beyond those listed under “ABSOLUTE MAXIMUM RATINGS” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
- 2) This particular frame decreases the total thermal resistance of the package and increases its ability to dissipate power when an appropriate area of copper on the printed circuit board is available for heat-sinking.

CAUTION

This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. SUMSEMI recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications. SUMSEMI reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time. Please contact SUMSEMI sales office to get the latest datasheet.

ELECTRICAL CHARACTERISTICS

($V_{IN} = 5\text{ V}$, $V_{OUT} = 2.5\text{ V}$, $L = 2.2\text{ }\mu\text{H}$, $C_{OUT} = 10\text{ }\mu\text{F}$, $T_A = 25^\circ\text{C}$, unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IN}	Input Voltage Range		2.5	5	6	V
OVP	Over Voltage Protection			6.5		V
V_{UVLO}	Input UVLO threshold	V_{IN} rising		2.3	2.45	V
V_{HYS}	UVLO hysteresis			0.18		V
I_Q	Quiescent Current	$I_{OUT} = 0$, $V_{FB} = V_{REF} * 105\%$		35	65	μA
I_{SHDN}	Shutdown Current	$V_{EN} = 0\text{ V}$		0.1	10	μA
V_{REF}	Feedback Reference Voltage		0.588	0.600	0.612	V
$R_{DS(ON),P}$	PFET RON			110		m Ω
$R_{DS(ON),N}$	NFET RON			72		m Ω
I_{LIM}	PFET Current Limit	$V_{OUT} = 2.5\text{ V}$	3			A
I_{DIS}	SW Discharge current	$V_{EN} = 0\text{ V}$		160		mA
V_{ENH}	EN rising threshold		1.5			V
V_{ENL}	EN falling threshold				0.4	V
I_{EN_LK}	EN Leakage Current			0.01	2.0	μA
V_{PG_TH}	Power Good Threshold	PG low, FB falling		90		%
		PG high, FB rising		90		%
I_{PG_SINK}	Power Good Sink Current				2.0	mA
F_{OSC}	Oscillator Frequency	$I_{OUT} = 0.5\text{ A}$		1.5		MHz
		$V_{OUT} = 0\text{ V}$		400		kHz
t_{ON_MIN}	Min ON Time			60		ns
D_{MAX}	Max Duty Cycle		100			%
T_{SS}	Soft Start Time			500		μs
T_{SD}	Thermal Shutdown Temperature			165		$^\circ\text{C}$
T_{HYS}	Thermal Shutdown Hysteresis			25		$^\circ\text{C}$

FUNCTIONAL DESCRIPTION

Input Protection

The chip has an under-voltage lockout function, which ensures that the chip will not start until the battery voltage reach the specified voltage, and a hysteresis function is set for UVLO to ensure that noise on the power supply does not cause system failure. When the input voltage is less than 2.5V, the chip stops working and is in a protection state. The under-voltage lockout circuit of the chip has a simple structure, low power consumption, and only a very small static power consumption, which does not affect the efficiency of the power supply, hardly increases the burden on the chip cooling system and affects the stability of the system, and enables the system to be able to work properly.

Output Protection

The chip has an output over-voltage protection function, which prevents the power supply from inputting too high voltage to the more sensitive devices. Once the power has been switched on, the OVP will continue to working and cannot be switched off manually. If the output voltage exceeds the OVP setting value, the power output will be switched off, thus protecting the device from damage caused by excessive voltage.

The chip has an output over-current protection function, which prevents the load from being burned out due to excessive output current. When the output current exceeds the OCP setting value, the power supply output will be switched off.

The chip has a short-circuit protection function. When the output terminal is short-circuited, the chip will be switched off and the output will be stopped to avoid circuit damage.

Soft Start

During the power-up of the chip, the output voltage rises from zero to the maximum value. Due to the effect of negative feedback, the duty cycle of the PWM control signal of the power tube changes from the maximum value and gradually decreases until the circuit is stable. Due to the existence of output filter capacitors in the circuit, it is easy to generate inrush current when charging the capacitors. At this time, a large current will flow through the power tube, which is easy to burn the circuit system. Therefore, there is a voltage soft start in the chip, and the output voltage gradually increases from 0V to the rated output voltage during power-on, reducing the inrush current received by the load.

Power Good (only for SUM5202KA6)

The PG pin is an open-drain output state. When the chip is just powered on, the PG pin is in a high-impedance output state. When the output voltage is normal, the PG pin is a low impedance output. Connect a pull-up resistor to this pin to output a high level just after power-on, and output a low level after the output is stable

FB Adjustment

FB is feed-back, the output voltage is divided by the resistor and then connected to this pin. The feedback voltage will be connected to the internal comparator of the chip and compared with the internal reference voltage (0.6 V). The result of the comparison will control the change of the duty cycle, so as to achieve the purpose of stabilizing the voltage.

PWM/PFM Working Mode

The PWM/PFM hybrid control method is to stabilize the output voltage by changing the width and pulse frequency of the square wave. At full load, PWM is used, which has relatively high efficiency and a wide range of duty cycles. The PFM work mode is used at light load, which has higher efficiency than PWM.

APPLICATION INFORMATION

Setting Output Voltages

The output voltage is set by an external resistor divider according to Equation:

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R_H}{R_L}\right) = 0.6 \text{ V} \times \left(1 + \frac{R_H}{R_L}\right)$$

There is no strict requirement for the feedback resistor. An R_H value greater than 10 k Ω is reasonable for most applications. R_L must not be higher than 100 k Ω to achieve high efficiency at light load while providing acceptable noise sensitivity.

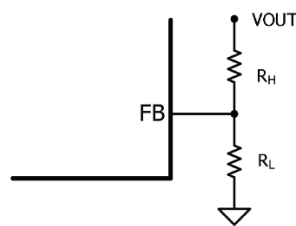


Figure 2 Feedback Network

Selecting the Inductor

Most applications work best with a 1 ~ 2.2 μH inductor. Select an inductor with a DC resistance less than 50m Ω to optimize efficiency. a high-frequency, switch-mode power supply with a magnetic device produces a strong electronic magnetic inference in the system. Any shield inductor, are ideal for applications as they can decrease the influence effectively.

For most designs, estimate the inductance value with Equation:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_s}$$

Where ΔI_L is the inductor ripple current.

Choose an inductor current that is approximately 30% of the maximum load current. The maximum inductor peak current can be calculated with Equation:

$$I_{PEAK} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Selecting the Input Capacitor

A typical X5R or better grade ceramic capacitor with 6.3 V rating and no less than 10 μF capacitance is recommended. To minimize the potential noise problem, we place this ceramic capacitor really close to the IN and GND pins. Care should be taken to minimize the loop area formed by C_{IN} , and IN/GND pins.

When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent an excessive voltage ripple at the input. The input voltage ripple caused by the capacitance can be estimated with Equation:

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_s \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Selecting the Output Capacitor

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. Estimate the output voltage ripple with Equation:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_s \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_s \times C_{OUT}}\right)$$

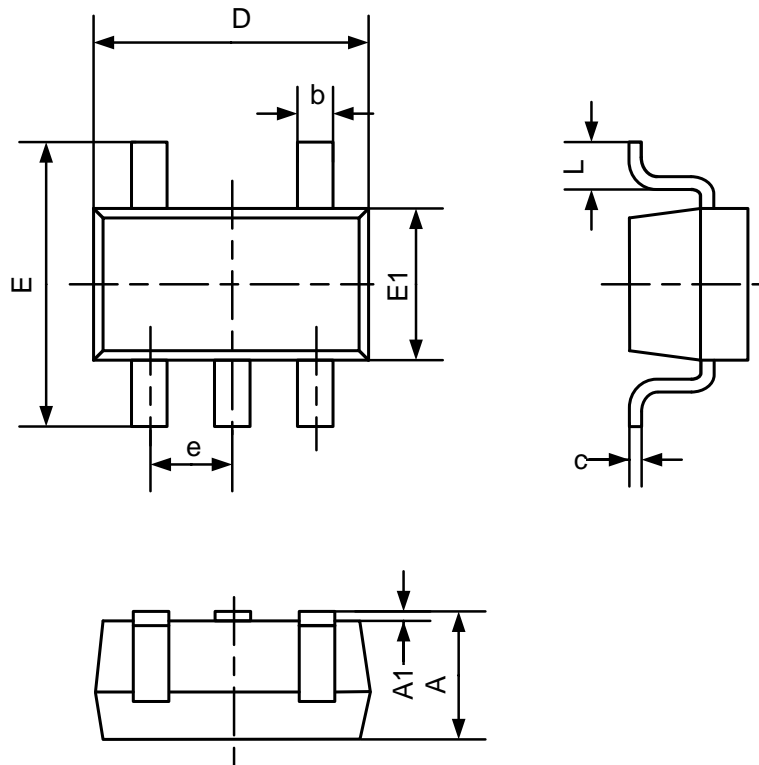
Where L is the inductor value, and RESR is the equivalent series resistance (ESR) value of the output capacitor.

For the best performance, it is recommended to use X5R or better grade ceramic capacitor with 6.3 V rating and no less than 10 μ F capacitance.

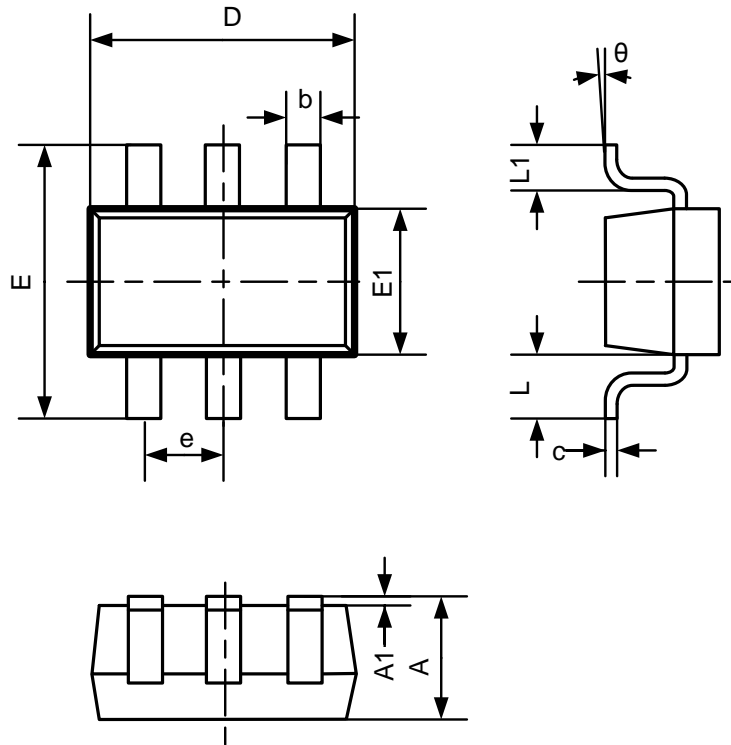
PCB Layout Guidelines

Efficient layout of the switching power supplies is critical for stable operation. For best results, follow the guidelines below.

1. Place the high-current paths (GND, IN, and SW) very close to the device with short, direct, and wide traces.
2. Place the input capacitor as close to IN and GND as possible.
3. Place the external feedback resistors next to FB.
4. Keep the switching node SW short and away from the feedback network.
5. Keep the V_{OUT} sense line as short as possible or away from the power inductor, especially the surrounding inductor.

PACKAGE OUTLINE
SOT23-5


Symbol	Dimensions In Millimeters	
	Min	Max
A	1.00	1.40
A1	0.00	0.10
b	0.30	0.50
c	0.10	0.25
D	2.70	3.10
E	2.50	3.10
E1	1.50	1.80
e	0.95BSC	
L	0.20	

PACKAGE OUTLINE
SOT23-6


Symbol	Dimensions In Millimeters	
	Min	Max
A	1.050	1.250
A1	0.000	0.100
b	0.300	0.500
c	0.100	0.200
D	2.670	3.170
E	2.500	3.100
E1	1.350	1.850
e	0.950BSC	
L	0.300	0.600
θ	0°	8°