
4.5V to 38V Input, 3A Synchronous Step-Down Regulator

DESCRIPTION

The SUM5884 is a highly integrated, wide input voltage, 3 A output synchronous buck convertor. The device is optimized to operate with minimum external component counts and also optimized to achieve low standby current.

This convertor adopts adaptive constant-on-time (ACOT) structure, and provides a fast transient response. It also supports both low-equivalent series resistance (ESR) output capacitors and ultra-low ESR ceramic capacitors with no external compensation components. During light load operation, SUM5884 operates in pulse frequency modulation (PFM) mode, which maintains high efficiency.

SUM5884 is available in ESOP-8 package.

FEATURES

- 3 A Converters Integrated 130 m Ω and 100 m Ω FET
- ACOT mode control with fast transient response
- Input Voltage Range: 4.5 V ~ 38 V
- Output Voltage Range: V_{FBTH} to 7.0 V
- FB voltage is 0.923 V (TYP)
- PFM mode during light load operation
- 600 KHz Switching Frequency
- Low Shutdown Current Less than 5 μ A
- Start-up from Pre-Biased Output Voltage
- Cycle-by-Cycle Over-current Limit
- Hiccup-mode Over-current Protection
- Non-Latch UVP and TSD Protections
- Fixed Soft Start: 1.0 ms
- Package: ESOP-8

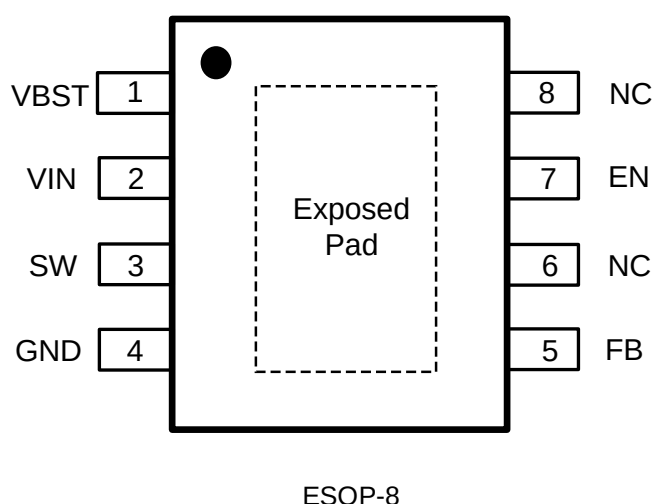
APPLICATIONS

- Digital TV Power Supply and Surveillance
- Disc Players
- Networking Home Terminal
- Digital Set Top Box

ORDER INFORMATION

Model	Package	Ordering Number	Packing Option
SUM5884	ESOP-8	SUM5884ES8	Tape and Reel, 2500

PIN CONFIGURATION (Top View)

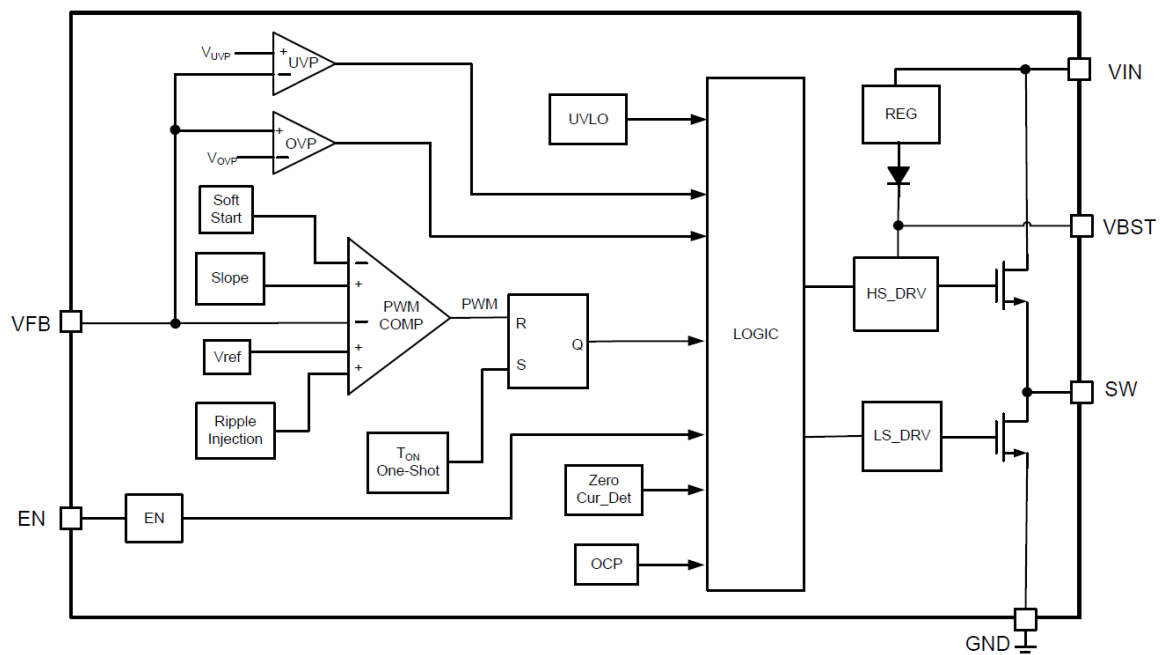


PIN FUNCTION

Pin Name	Pin No.	I/O	Description
VBST	1	O	Power supply of high-side NFET control circuit. Connect 0.1 μ F capacitor between VBST and SW pins.
VIN	2	I	Input voltage supply pin, also the drain terminal of high-side power NFET.
SW	3	O	Switch node connection between low-side NFET and high-side NFET.
GND	4		Ground pin of controller circuit, as well as source terminal of low-side power NFET. Connect sensitive VFB to this GND at a single point.
FB	5	I	Output voltage feedback pin. Connect to output voltage with feedback resistor divider.
NC	6, 8		No connect.
EN	7	I	Enable pin. Must be pulled up to enable the device.
EP			Exposed Pad for heat dissipating, it is recommended to connect GND.

Note: The Exposed Pad must be connect with GND on Printed Circuit Board.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Overview

The SUM5884 is highly integrated, 3 A synchronous Buck converter. It employs adaptive constant on time (ACOT) mode, and supports low ESR output capacitors such as specialty polymer capacitors and multi-layer ceramic capacitors without complex external compensation circuits. The fast transient response of this device can reduce the output capacitance.

Adaptive On-Time Control and PWM Operation

The main control mode of SUM5884 is pulse width modulation (PWM) with ACOT structure. This control mode control can achieve pseudo-fixed frequency and stable operation with both low-ESR and ceramic output capacitors.

The high-side MOSFET is turned on at the beginning of each cycle. When one shot timer expires, the high-side power FET is turned off. This one shot duration is set proportional to input voltage, VIN, and inversely proportional to the output voltage, VO, to achieve pseudo-fixed frequency over the input voltage range, hence it is called adaptive constant on-time control. The one-shot timer is reset and the high-side power FET is turned on again when the feedback voltage falls below the reference voltage. An internal ramp is generated to emulate output ripple, eliminating the need for ESR of output capacitor.

Pulse Frequency Modulation

The SUM5884 is designed with pulse frequency modulation mode to achieve high efficiency during light load condition. As the output current decreases from heavy load condition, the inductor current also decreases and eventually comes to zero, which is the boundary between continuous conduction and discontinuous conduction modes. The low-side power FET is turned off when the zero inductor current is detected. As the load current further decreases the converter enters into discontinuous conduction mode. The on-time is almost the same as it was in the continuous conduction mode so that it takes longer time to discharge the output capacitor with smaller load

current to the level of the reference voltage. This makes the switching frequency lower, proportional to the load current, and keeps efficiency high in light load condition. The transition point to the light load operation $I_{OUT(LL)}$ current can be calculated in Equation 1.

$$I_{OUT(LL)} = \frac{1}{2 \times L \times f_{sw}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (1)$$

In PFM mode, each switching cycle is followed by a period of energy saving sleep time. The sleep time ends when the VFB voltage falls below the threshold voltage. As the output current decreases, the sleep time between switching pulses increases.

Soft Start and Pre-Biased Soft Start

The SUM5884 is designed with an internal 1ms soft-start. When the VIN is plugged in and the EN pin becomes high, the reference voltage of PWM comparator begins to rise from zero.

If the output capacitor is pre-biased at start-up, the device begins to switch and start ramping up only after the internal reference voltage becomes greater than the feedback voltage VFB. This scheme ensures that the convertors ramp up smoothly into regulation point.

Current Protection

The over-current limit (OCL) is implemented by using cycle-by-cycle valley detect control circuit. The switch current is monitored by measuring the low-side FET drain to source voltage during its on-state. This voltage is proportional to the switch current. To improve accuracy, the voltage sensing is temperature compensated.

During the on-state of high-side FET, the switch current increases at a linear rate determined by VIN, VOUT, and the inductor value. During the on time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current I_{OUT} . If the monitored current is above the OCL level, the convertor keeps low-side FET on and prevents the creation of a new set pulse, even the voltage feedback loop requires one, until the current level decreases to OCL level or lower. In next switching cycles, the on-time is set to a fixed value and the current is monitored in the same manner.

The load current is higher than the over-current threshold by one half of the peak-to-peak inductor ripple current. Also, when the current is being limited, the output voltage tends to fall as the load current is higher than the current available from the convertor. This may cause the output voltage to fall. When the VFB voltage falls below the UVP threshold voltage, the UVP comparator detects it. And then, the device will shut down after the UVP delay time and re-start after the hiccup time (typically 12 ms). When the over current condition is removed, the output voltage returns to the regulated value.

Under-voltage Lockout (UVLO) Protection

UVLO protection monitors the internal regulator voltage. When the voltage is lower than UVLO threshold voltage, the device is shut off. When input voltage increases up to the upper threshold of UVLO, it begins to switch.

Thermal Shutdown

The device monitors the temperature of itself. If the temperature exceeds the threshold value (typically 170°C), the device is shut off. When the temperature falls to about 140°C or below, the convertor begins to switch.

Standby Operation

When the SUM5884 is operating in either normal CCM or PFM, they may be placed in standby by pulling the EN pin to low.

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted)

Symbol	Parameters	Min	Max	Unit
V _I	VIN Voltage Range	-0.3	40	V
	EN Voltage Range	-0.3	40	V
	VBST Voltage Range	-0.3	44	V
	VBST(10 ns transient) Voltage Range	-0.3	46	V
	VBST(VS SW) Voltage Range	-0.3	6.5	V
	VFB Voltage Range	-0.3	6.5	V
	SW Voltage Range	-2	40	V
	SW (10ns transient)	-3.5	42	V
V _{ESD}	Human Body Model (JEDEC JS-001)	±2000		V
	Charged Device Model (JESD22-C101)	±1000		V
T _J	Junction Temperature	-40	+150	°C
T _{STG}	Storage Temperature	-65	+150	°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameters		Min	Typ	Max	Unit
V _{IN}	Supply Input Voltage Range (VIN)		4.5		38	V
V _I	Input Voltage Range	VBST	-0.1		42	
		VBST(10 ns transient)	-0.1		45	
		VBST (VS SW)	-0.1		6	
		EN	-0.1		38	
		VFB	-0.1		5.5	
		SW	-1.8		38	
		SW (10 ns transient)	-3.5		40	
T _J	Operating Junction Temperature		-40		125	°C
T _A	Ambient Temperature		-40		85	°C

ELECTRICAL CHARACTERISTICS

$V_{IN} = 12\text{ V}$, $T_A = -40^\circ\text{C} \sim 85^\circ\text{C}$, (unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Supply Current						
I _{IN}	Operating–non-switching Supply Current	V _{IN} current, EN = 5 V, V _{FB} = 1.0 V		300		μA
I _{IN_OFF}	Shutdown supply current	V _{IN} current, EN = 0 V		1.6	5	
Logic Threshold						
V _{ENH}	EN High-level Input Voltage		1.6			V
V _{ENL}	EN Low-level Input Voltage				0.8	
R _{EN}	EN Pin Resistance to GND	V _{EN} = 12 V	200	320	600	kΩ
V _{FB} Voltage and Discharge Resistance						
V _{FBTH}	V _{FB} Threshold Voltage	V _O = 1.05 V, I _O = 10 mA, PFM operation		930		mV
	V _{FB} Threshold Voltage	V _O = 1.05 V, Continuous mode operation	900	923	946	mV
I _{FB}	V _{FB} Input Current	V _{FB} = 1.0 V			0.1	μA
MOSFET						
R _{DS(ON)H}	High-side Switch Resistance	T _A = 25°C, V _{BST} – V _{SW} = 5V		130		mΩ
R _{DS(ON)L}	Low-side Switch Resistance	T _A = 25°C		100		mΩ
Current Limit						
I _{OCL}	Current Limit	DC current, V _{OUT} = 1.05 V, L ₁ = 2.2 μH	3.5	4.2	5.5	A
Thermal Shutdown						
T _{SDN}	Thermal Shutdown Threshold ⁽¹⁾	Shutdown temperature		170		°C
T _{SDN_HYS}		Hysteresis		30		
ON-Time Timer Control						
t _{OFF(MIN)}	Minimum off Time	V _{FB} = 0.5V		150		ns
Soft Start						
T _{SS}	Soft Start Time	Internal soft-start time		1.0		ms
Frequency						
F _{SW}	Switching Frequency	CCM mode		600		KHz
Output Under-voltage Protection						
V _{UVP}	Output UVP Threshold	Hiccup detect (H > L)		60		%
UVLO						
V _{UVLO}	UVLO Threshold	Wake up V _{IN} voltage		3.9	4.3	V
		Shutdown V _{IN} voltage	3.3	3.5		
		Hysteresis V _{IN} voltage		0.5		

Note1: Not production tested, design assurance.

APPLICATION AND IMPLEMENTATION

Note

Information in the following applications sections is not part of the ETEK component specification. ETEK does not warrant its accuracy or completeness and Customers should be responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

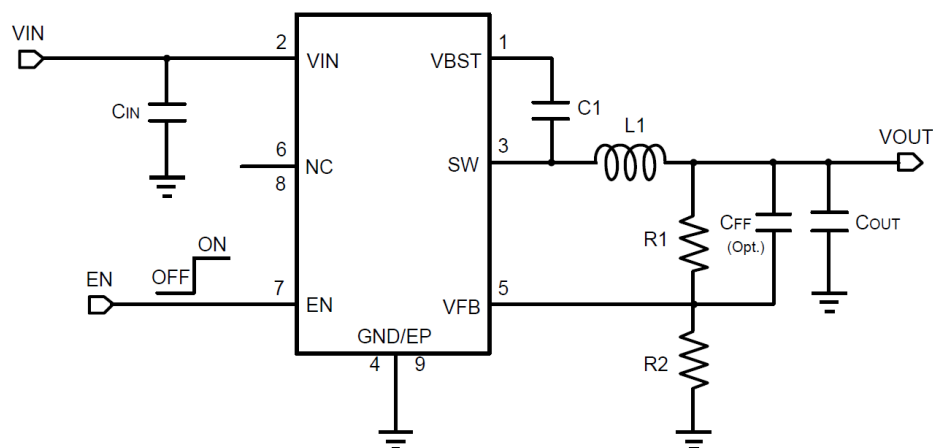
Application Information

SUM5884 is typical step-down DC-DC converter. It' s typically used to convert a higher DC voltage to a lower DC voltage with a maximum available output current of 3 A. The following design procedure can be used to select component values for the SUM5884.

Typical Application

The application schematic below was developed to meet the previous requirements. This circuit is available as the evaluation module (EVM). The sections provide the design procedure.

The figure shows SUM5884 converter schematics.



OUT=X.XV / 3 A Reference Design

Design Requirements

This table below shows the design parameters for this application.

Parameter	Example Value
Input voltage range	4.5 ~ 36 V
Output voltage	1.05 V
Transient response, 1.5 A load step	$\Delta V_{OUT} = \pm 2.5 \%$
Input ripple voltage	400 mV
Output ripple voltage	30 mV
Output current rating	3 A
Operating frequency	600 KHz

Detailed Design Procedure

Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the VFB pin. ETEK recommends using 1% tolerance or better divider resistors. Start by using Equation 2 to calculate VOUT.

If customers want to improve efficiency at very light loads, we recommend using larger value resistors. High value of resistor will be more susceptible to noise and voltage errors from the V_{FB} input current will be more noticeable.

$$V_{OUT} = 0.923 \times \left(1 + \frac{R1}{R2}\right) \quad (2)$$

Output Filter Selection

The LC filter used as the output filter has double pole at:

$$f_p = \frac{1}{2\pi\sqrt{L_{OUT} \times C_{OUT}}} \quad (3)$$

The overall loop gain is set by the output set-point resistor divider network and the internal gain of the device at low frequencies. The low frequency phase is 180°. At the output filter pole frequency, the gain rolls off at a -40 dB per decade rate and the phase drops rapidly. The inductor and capacitor for the output filter should be selected so that the double pole of Equation 3 is located below the high frequency zero but close enough that the phase boost provided by the high frequency zero provides adequate phase margin for a stable circuit.

Example for V_{FB} = 0.923 V

V _{OUT} (V)	R1(KΩ)	R2(KΩ)	L1(μH)	C1(nF)	C _{IN} (μF)	C _{OUT} (μF)	C _{FF} (pF) Opt.
1.0	0.83	10	2.2	100	22	22×2	CFF Chapter
1.2	3	10	2.2	100	22	22×2	CFF Chapter
1.5	6.25	10	2.2	100	22	22×2	CFF Chapter
1.8	9.5	10	2.2	100	22	22×2	CFF Chapter
2.5	17.1	10	2.2	100	22	22×2	CFF Chapter
3.3	25.7	10	3.3	100	22	22×2	CFF Chapter
5.0	44.2	10	4.7	100	22	22×2	CFF Chapter

The inductor peak to peak ripple current, peak current and RMS current are calculated using Equation 4, Equation 5, and Equation 6. The inductor saturation current rating must be greater than the calculated peak current and the RMS or heating current rating must be greater than the calculated RMS current.

$$I_{L\text{ P-P}} = \frac{V_{OUT}}{V_{IN(MAX)}} \times \frac{V_{IN(MAX)} - V_{OUT}}{L_O \times f_{sw}} \quad (4)$$

$$I_{L\text{ peak}} = I_O + \frac{I_{L\text{ P-P}}}{2} \quad (5)$$

$$I_{LO(RMS)} = \sqrt{I_O^2 + \frac{1}{12} I_{L\text{ P-P}}^2} \quad (6)$$

For this design example, the calculated peak current is 3.5 A and the calculated RMS current is 3.01 A. The inductor should be used with a peak current rating of 13 A and an RMS current rating of 9 A.

The capacitor value and ESR determines the amount of output voltage ripple. The SUM5884 is intended for use with ceramic or other low ESR capacitors. We recommend using values range from 20 μF to 68 μF . Equation 7 determines the required RMS current rating for the output capacitor.

$$I_{CO(RMS)} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{\sqrt{12} \times V_{IN} \times L_O \times f_{sw}} \quad (7)$$

Two 22 μF output capacitors are used for this design. The typical ESR is 2 m Ω each. The calculated RMS current is 0.286 A and each output capacitor is rated for 4 A.

Input Capacitor Selection

The SUM5884 requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. We recommend a ceramic capacitor over 10 μF for the decoupling capacitor. An additional 0.1 μF capacitor (C3) from pin 3 to ground is optional to provide additional high frequency filtering. The capacitor voltage rating needs to be greater than the maximum input voltage.

Bootstrap Capacitor Selection

A 0.1 μF ceramic capacitor must be connected between the VBST to SW pin for proper operation. We recommend using a ceramic capacitor.

Power Supply Recommendations

SUM5884 is designed to operate from input supply voltage in the range of 4.5 V to 38 V. Buck converters require the input voltage to be higher than the output voltage for proper operation. The maximum recommended operating duty cycle is 75%. Using that criteria, the minimum recommended input voltage is $V_O/0.75$.

APPLICATION CURVES

$V_{IN} = 12\text{ V}$ (unless otherwise noted)

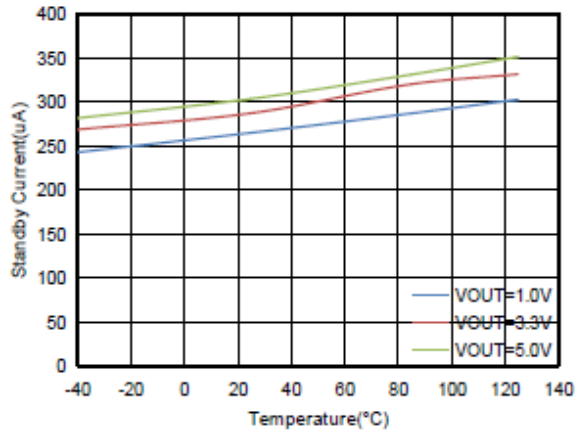


Figure1. Standby Current vs Temperature

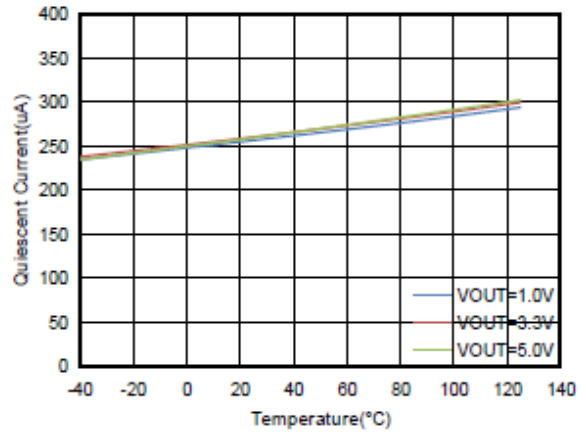


Figure2. Quiescent Current vs Temperature

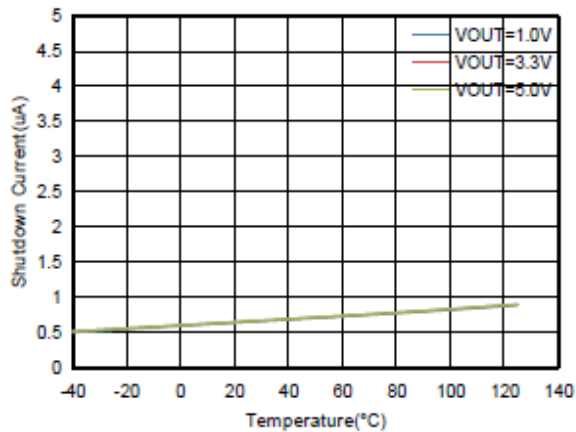


Figure3. Shutdown Current vs Temperature

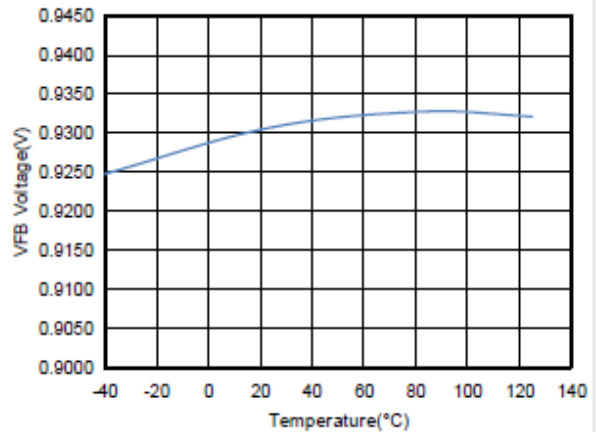


Figure4. VFB Voltage vs Temperature
IOUT=2A

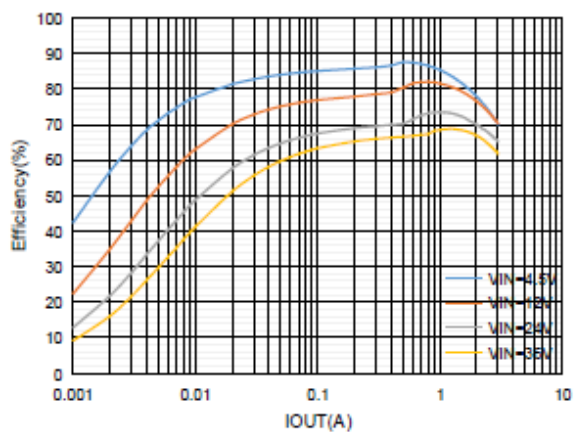


Figure5. Efficiency VOUT=1.0V

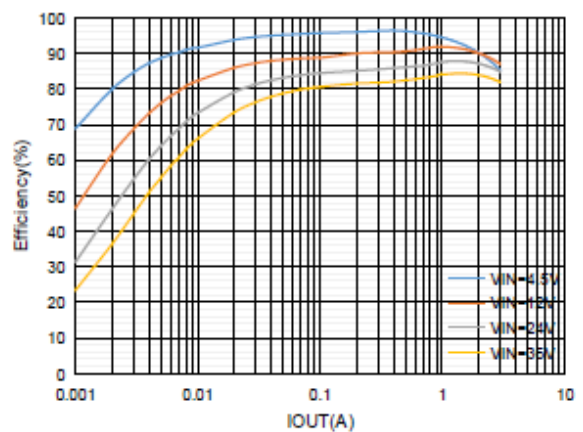
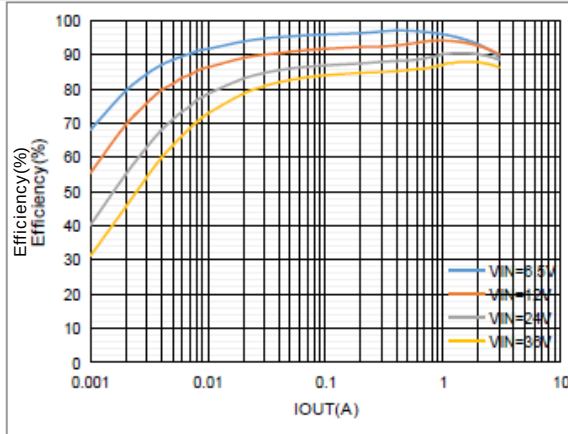
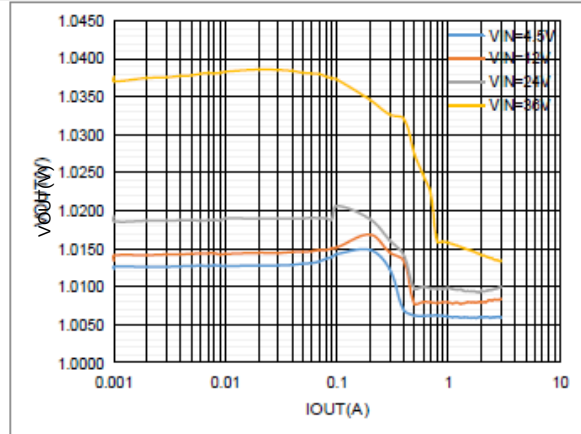
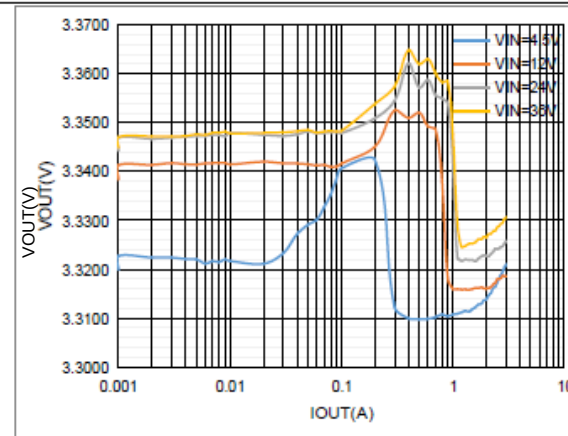
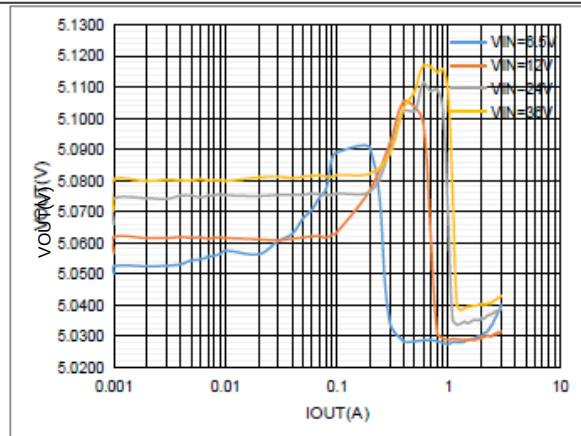
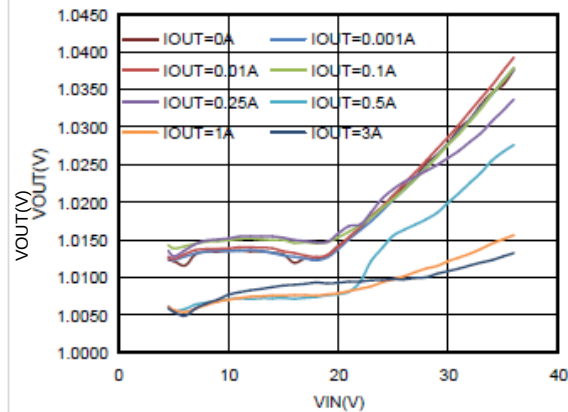
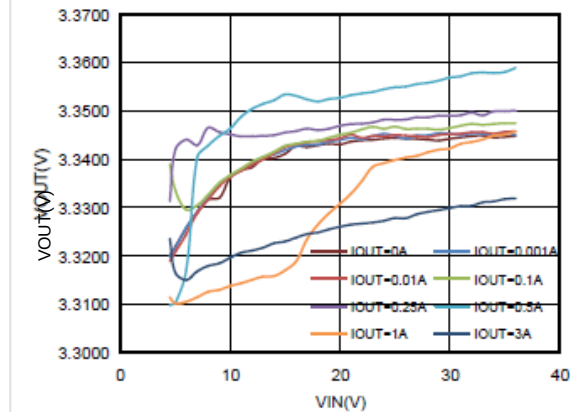


Figure6. Efficiency VOUT=3.3V


Figure7. Efficiency $V_{OUT}=5.0V$

Figure8. Load Regulation, $V_{OUT}=1.0V$

Figure9. Load Regulation, $V_{OUT}=3.3V$

Figure10. Load Regulation, $V_{OUT}=5.0V$

Figure11. Line Regulation, $V_{OUT}=1.0V$

Figure12. Line Regulation, $V_{OUT}=3.3V$

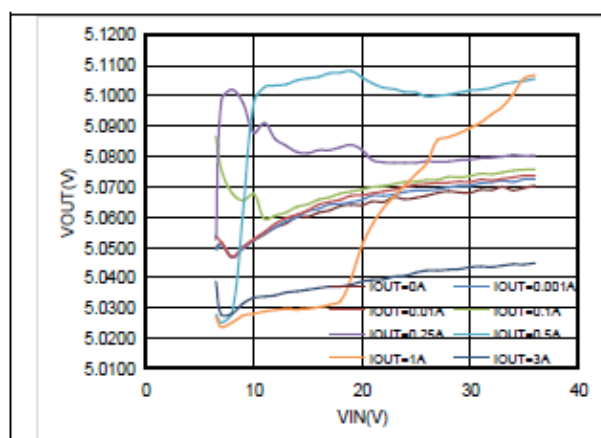
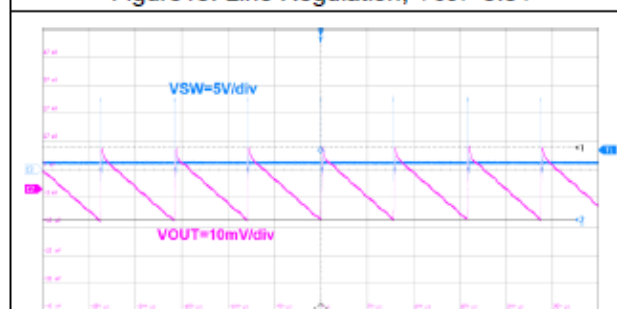
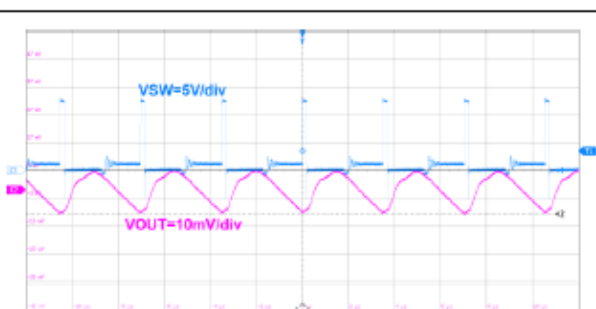


Figure13. Line Regulation, $V_{OUT}=5.0V$



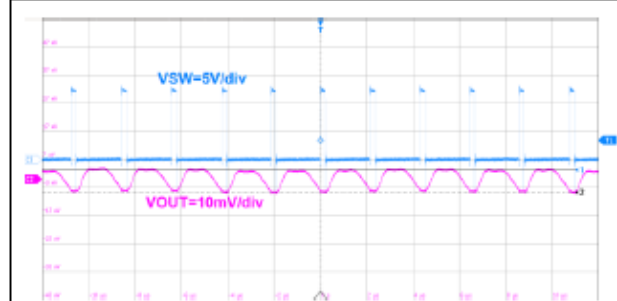
50us/div $V_{OUT}=1.0V$ $I_{OUT}=0.01A$

Figure14. Output Ripple



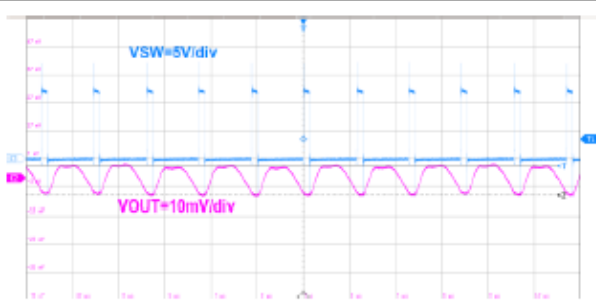
2us/div $V_{OUT}=1.0V$ $I_{OUT}=0.25A$

Figure15. Output Ripple



2us/div $V_{OUT}=1.0V$ $I_{OUT}=1.0A$

Figure16. Output Ripple



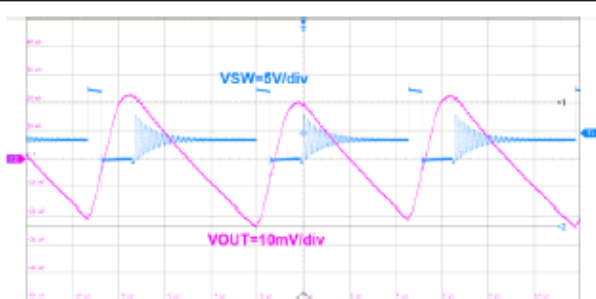
2us/div $V_{OUT}=1.0V$ $I_{OUT}=3.0A$

Figure17. Output Ripple



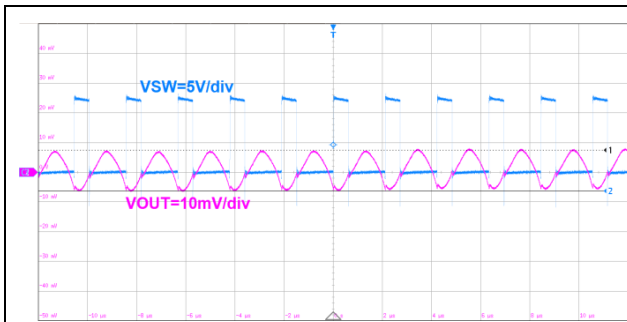
50us/div $V_{OUT}=3.3V$ $I_{OUT}=0.01A$

Figure18. Output Ripple



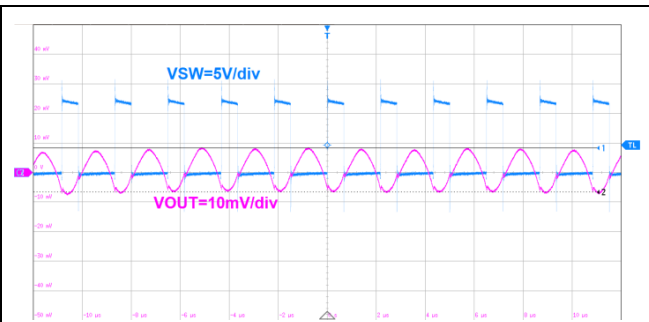
2us/div $V_{OUT}=3.3V$ $I_{OUT}=0.25A$

Figure19. Output Ripple



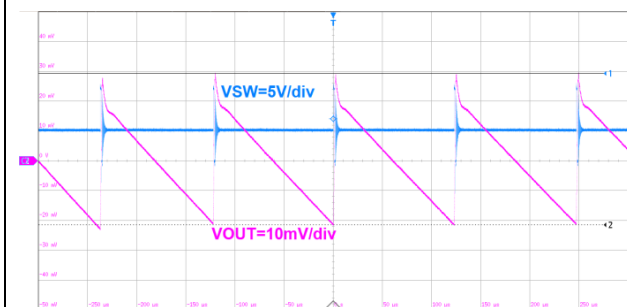
2us/div $V_{OUT}=3.3V$ $I_{OUT}=1.0A$

Figure20. Output Ripple



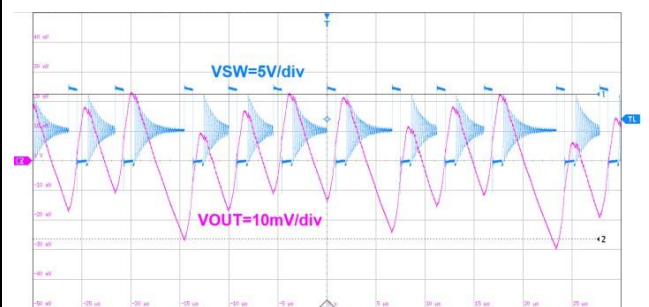
2us/div $V_{OUT}=3.3V$ $I_{OUT}=3.0A$

Figure21. Output Ripple



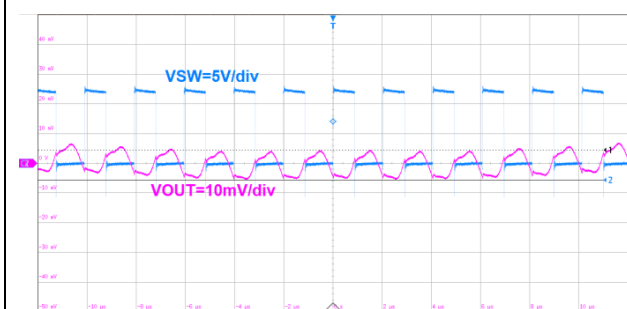
50us/div $V_{OUT}=3.3V$ $I_{OUT}=0.01A$

Figure22. Output Ripple



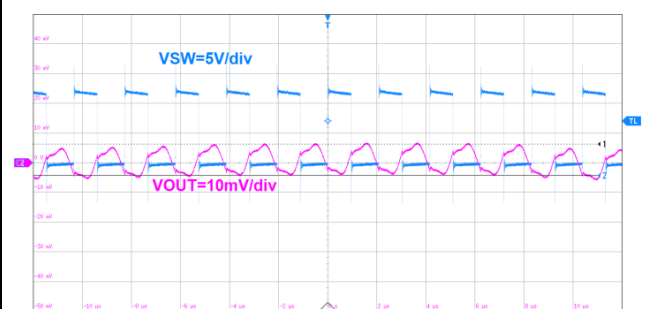
5us/div $V_{OUT}=3.3V$ $I_{OUT}=0.25A$

Figure23. Output Ripple



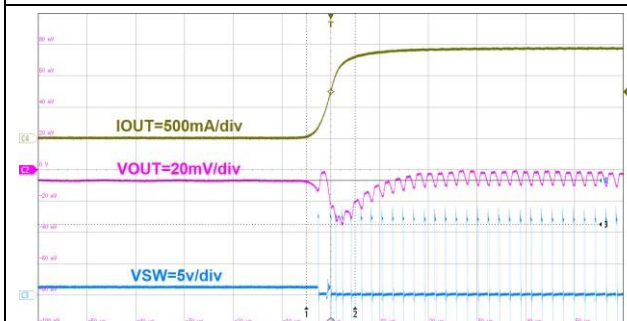
2us/div $V_{OUT}=3.3V$ $I_{OUT}=1.0A$

Figure24. Output Ripple



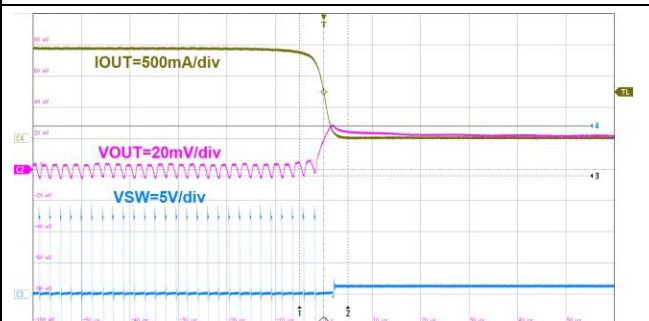
2us/div $V_{OUT}=3.3V$ $I_{OUT}=3.0A$

Figure25. Output Ripple



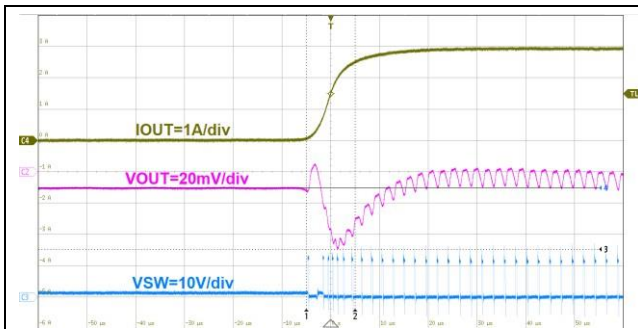
10us/div $V_{OUT}=1.0V$ $I_{OUT}=0A$ to $1.5A$

Figure26. Load Transient

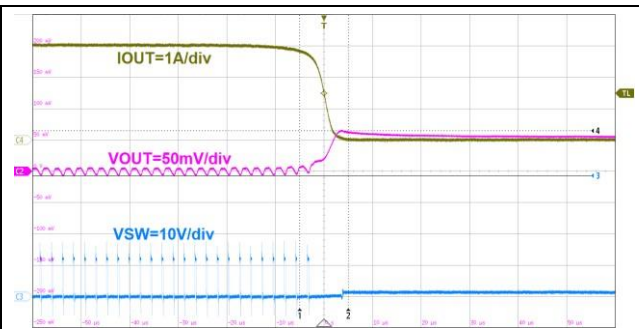


10us/div $V_{OUT}=1.0V$ $I_{OUT}=1.5A$ to $0A$

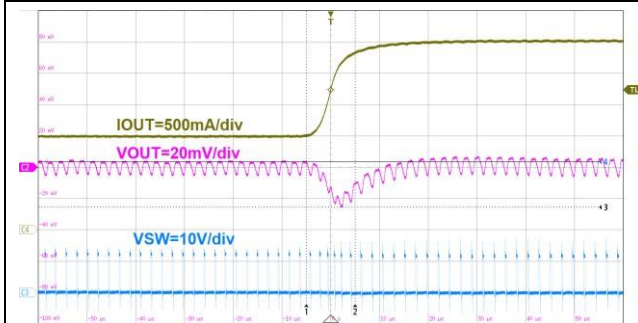
Figure27. Load Transient



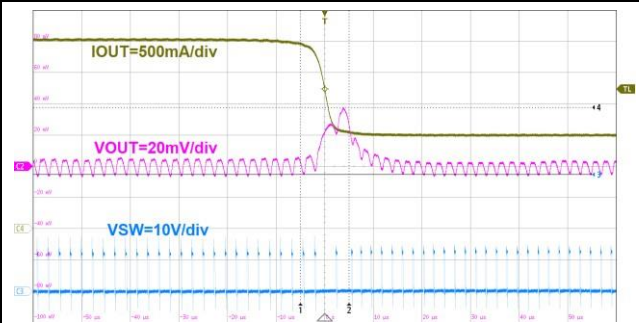
10us/div $V_{OUT}=1.0V$ $I_{OUT}=0A$ to $3A$
Figure28. Load Transient



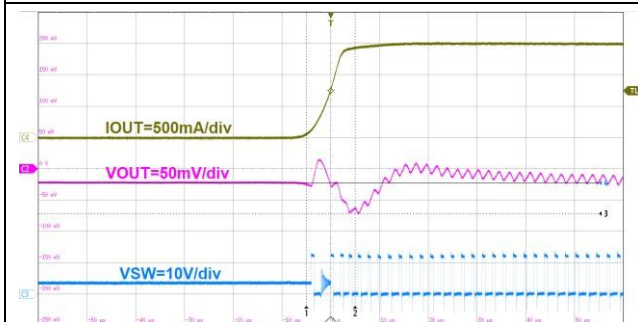
10us/div $V_{OUT}=1.0V$ $I_{OUT}=3A$ to $0A$
Figure29. Load Transient



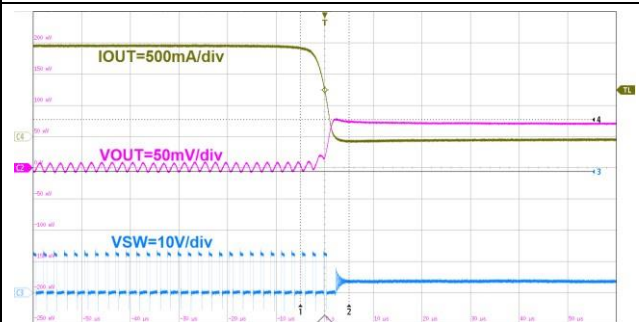
10us/div $V_{OUT}=1.0V$ $I_{OUT}=1.5A$ to $3A$
Figure30. Load Transient



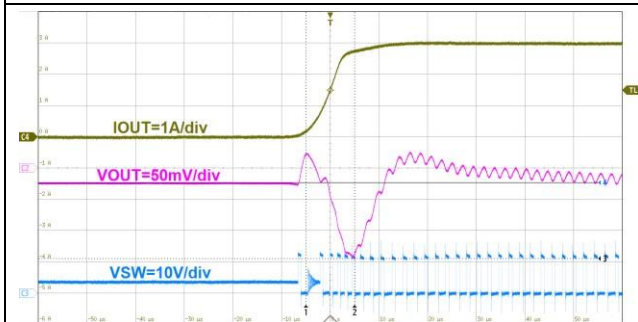
10us/div $V_{OUT}=1.0V$ $I_{OUT}=3A$ to $1.5A$
Figure31. Load Transient



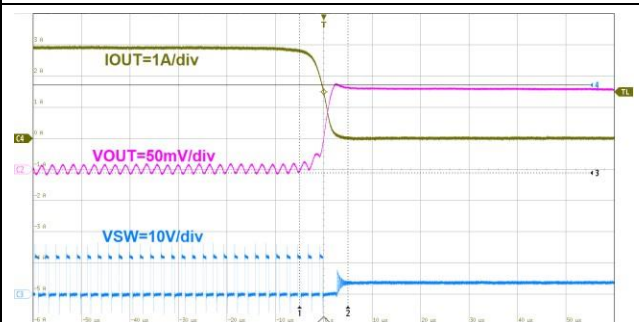
10us/div $V_{OUT}=3.3V$ $I_{OUT}=0A$ to $1.5A$
Figure32. Load Transient



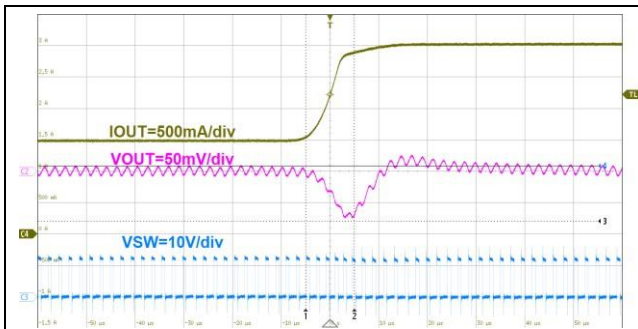
10us/div $V_{OUT}=3.3V$ $I_{OUT}=1.5A$ to $0A$
Figure33. Load Transient



10us/div $V_{OUT}=3.3V$ $I_{OUT}=0A$ to $3A$
Figure34. Load Transient

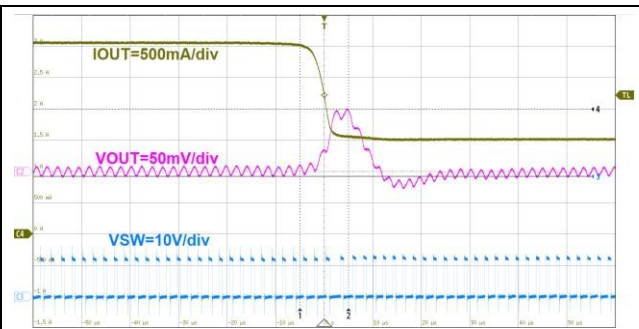


10us/div $V_{OUT}=3.3V$ $I_{OUT}=3A$ to $0A$
Figure35. Load Transient



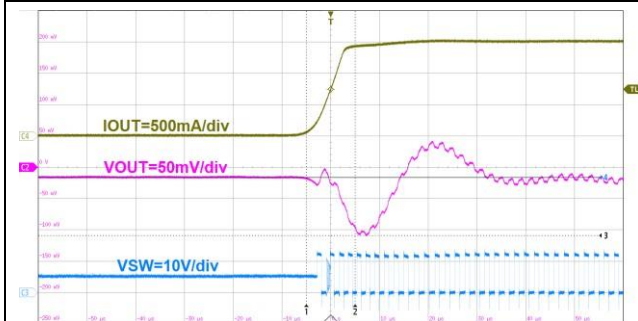
10us/div $V_{OUT}=3.3V$ $I_{OUT}=1.5A$ to $3A$

Figure36. Load Transient



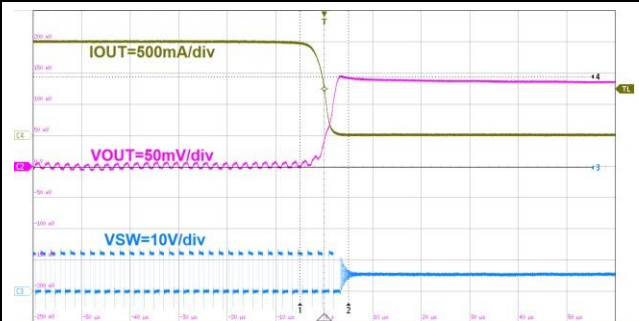
10us/div $V_{OUT}=3.3V$ $I_{OUT}=3A$ to $1.5A$

Figure37. Load Transient



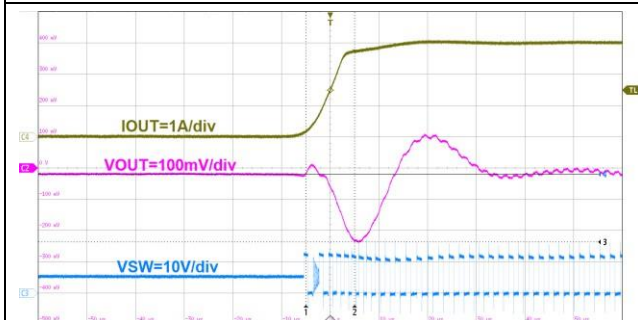
10us/div $V_{OUT}=5.0V$ $I_{OUT}=0A$ to $1.5A$

Figure38. Load Transient



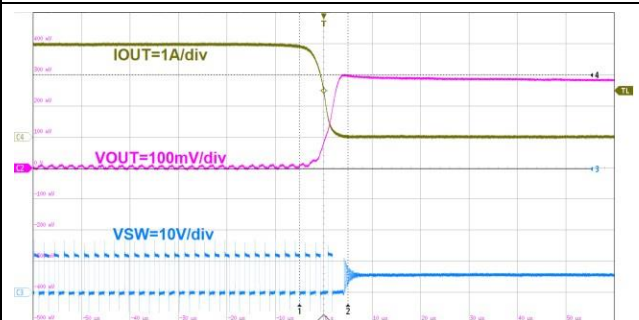
10us/div $V_{OUT}=5.0V$ $I_{OUT}=1.5A$ to $0A$

Figure39. Load Transient



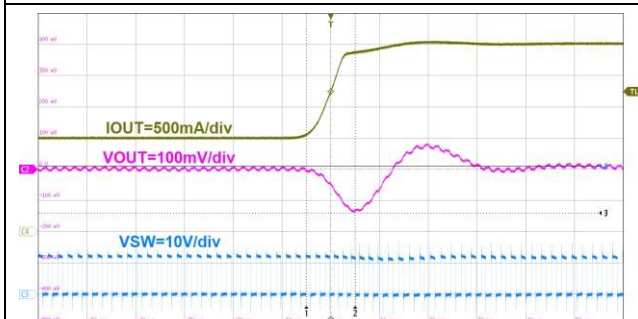
10us/div $V_{OUT}=5.0V$ $I_{OUT}=0A$ to $3A$

Figure40. Load Transient



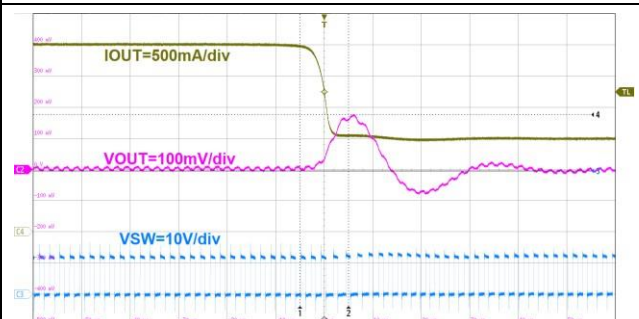
10us/div $V_{OUT}=5.0V$ $I_{OUT}=3A$ to $0A$

Figure41. Load Transient



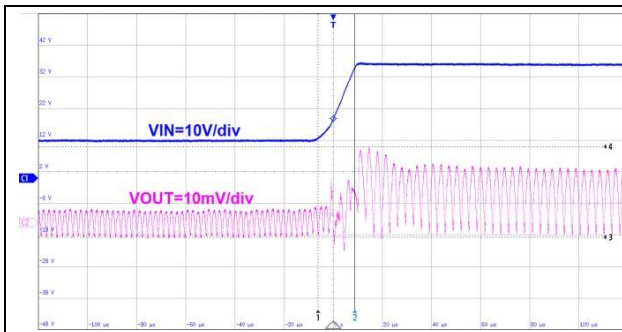
10us/div $V_{OUT}=5.0V$ $I_{OUT}=1.5A$ to $3A$

Figure42. Load Transient

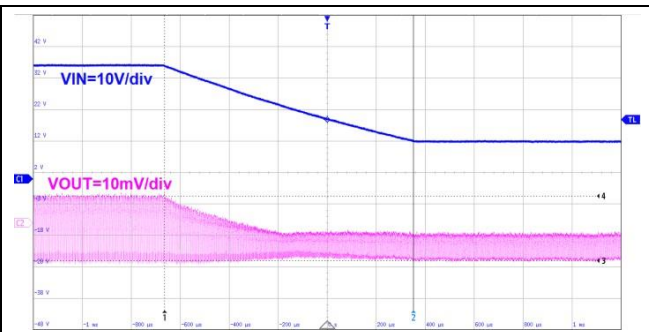


10us/div $V_{OUT}=5.0V$ $I_{OUT}=3A$ to $1.5A$

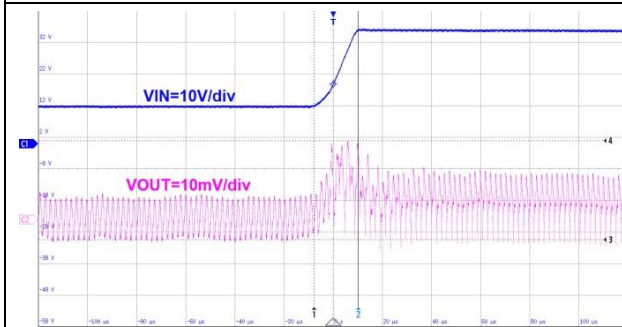
Figure43. Load Transient



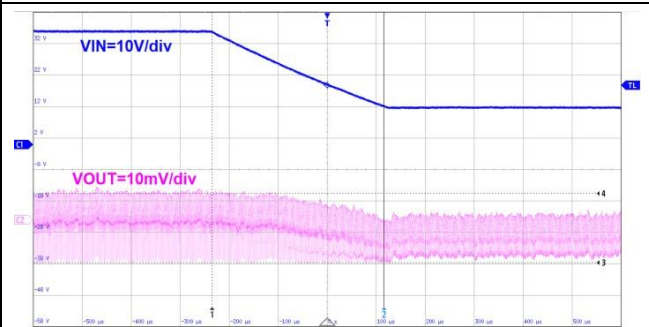
20us/div $V_{IN}=12V$ to $36V$ $V_{OUT}=1.0V$ $I_{OUT}=1.5A$
Figure44. Line Transient



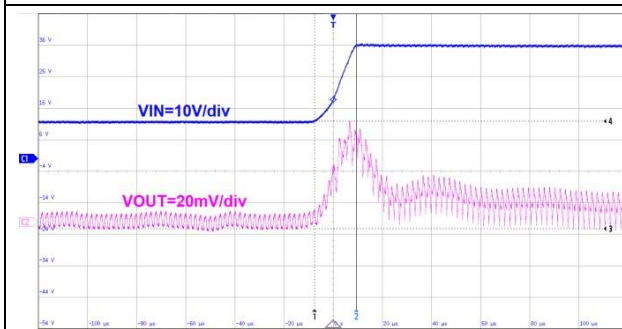
200us/div $V_{IN}=36V$ to $12V$ $V_{OUT}=1.0V$ $I_{OUT}=1.5A$
Figure45. Line Transient



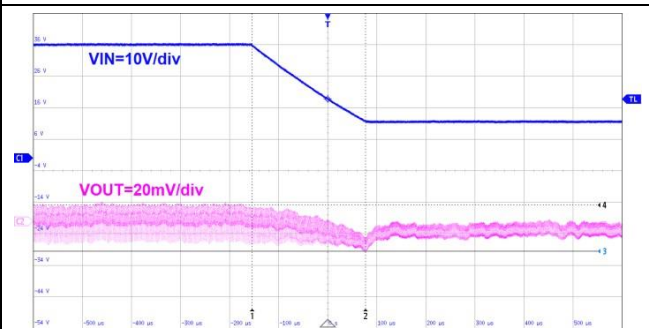
20us/div $V_{IN}=12V$ to $36V$ $V_{OUT}=3.3V$ $I_{OUT}=1.5A$
Figure46. Line Transient



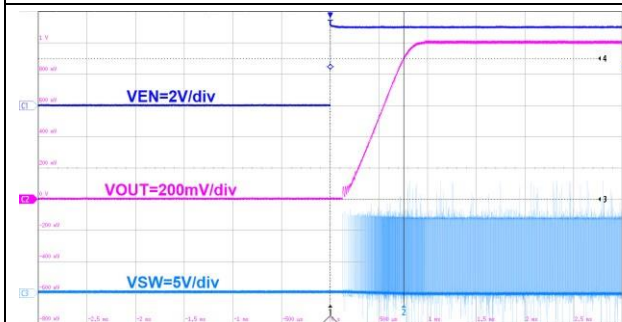
100us/div $V_{IN}=36V$ to $12V$ $V_{OUT}=3.3V$ $I_{OUT}=1.5A$
Figure47. Line Transient



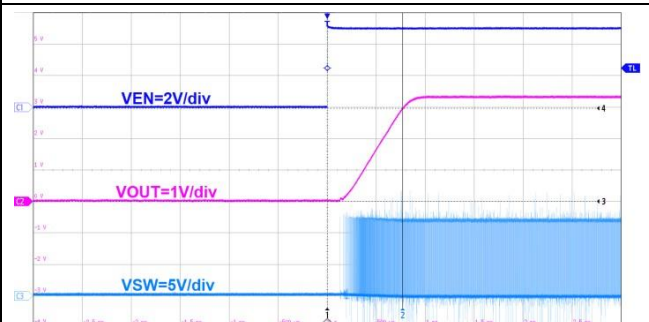
20us/div $V_{IN}=12V$ to $36V$ $V_{OUT}=5.0V$ $I_{OUT}=1.5A$
Figure48. Line Transient



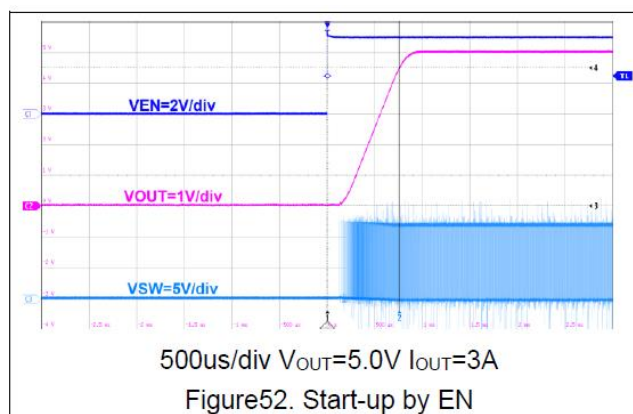
100us/div $V_{IN}=36V$ to $12V$ $V_{OUT}=5.0V$ $I_{OUT}=1.5A$
Figure49. Line Transient



500us/div $V_{OUT}=1.0V$ $I_{OUT}=3A$
Figure50. Start-up by EN

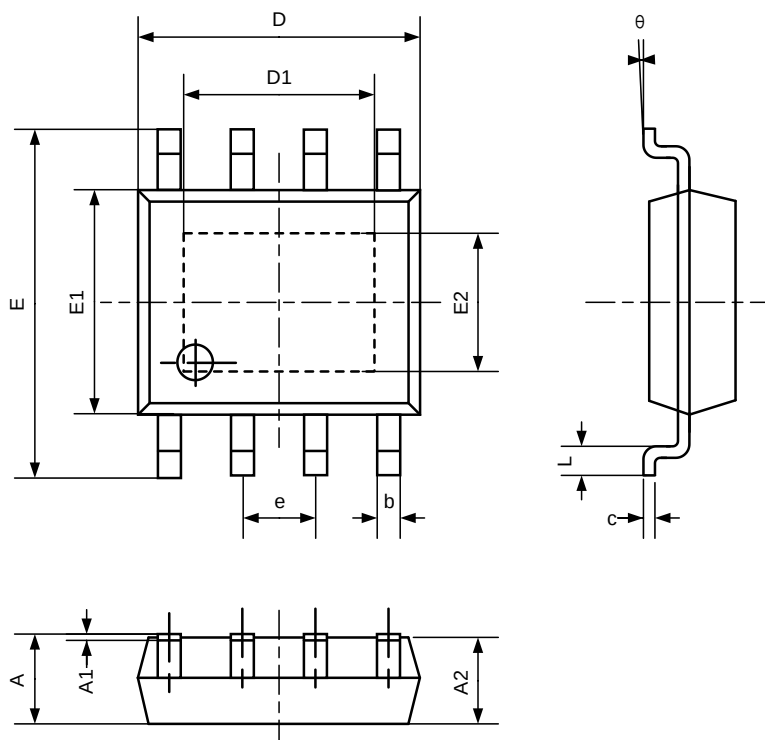


500us/div $V_{OUT}=3.3V$ $I_{OUT}=3A$
Figure51. Start-up by EN



PACKAGE OUTLINE

ESOP-8



Symbol	Dimensions In Millimeters	
	Min	Max
A	1.350	1.700
A1	0.000	0.100
A2	1.350	1.550
b	0.330	0.510
c	0.170	0.250
D	4.700	5.100
D1	3.202	3.402
E	5.800	6.200
E1	3.800	4.000
E2	2.313	2.513
e	1.270BSC	
L	0.400	1.270
θ	0°	8°